# POWER AND PERFORMANCE OPTIMIZATION OF NEGATIVE CAPACITANCE TRANSISTOR CIRCUITS

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**POWER AND PERFORMANCE OPTIMIZATION OF NEGATIVE CAPACITANCE TRANSISTOR CIRCUITS**

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In the end, it's not going to matter how many breaths you took, but how many moments took your breath away.

*Shing Xiong*

This work is dedicated to my beloved parents and brother.

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## TABLE OF CONTENTS

## LIST OF TABLES

## LIST OF FIGURES

## SUMMARY

Negative Capacitance Field Effect Transistor (NCFET) is an emerging technology solution for achieving extremely low power and high performance. The negative capacitance exhibited by the ferroelectric layer of the transistor results in very high effective gate capacitance leading to electrostatic voltage amplification. In other words, the internal gate voltage is extremely amplified facilitating low sub-threshold slopes and enhanced drain-currents. Therefore, NCFET tremendously reduces power consumption by enabling extremely low voltage operation. Whereas the enhanced current behavior of NCFET enables extremely high-performance improvement.

The NCFET characteristics depend on various parameters such as the ferroelectric properties and operating voltage. In this work, the effects of ferroelectric parameters on device characteristics are exhaustively analyzed at various operating voltages. The power and performance exploration is then extended to logic gate and full-chip designs. The characteristics of several logic gates are carefully studied to associate observed power-performance effects with root-cause parameters. Two full-chip benchmarks, a cell-dominated and a wire-dominated design are used for full-chip analysis in order to obtain a generic understanding of the negative capacitance effects. The multi-level comprehensive NCFET analysis provides a counter-intuitive design guideline: NCFET with the lowest sub-threshold slope may not provide minimum power consumption or maximum performance. Under certain conditions, such NCFETs actually deteriorate power consumption and performance compared to NCFETs with a higher sub-threshold slope.

The NCFET power analysis shows that power consumption depends on a combination of factors such as operating voltage, NCFET transfer characteristics, and threshold voltage in addition to sub-threshold slope. Further, the comprehensive multi-voltage multi-level analysis also reveals a notion of optimal ferroelectric parameter and operating voltage combination for iso-performance maximum power reduction. An NCFET with certain fer-

roelectric properties can be associated with an optimal voltage and for a given operating voltage a certain set of optimal ferroelectric parameters provide maximum power reduction. At a given operating voltage, the feasible NCFETs with low current enhancement provide maximum power reduction. The optimal NCFETs are also influenced by design type as the wire-dominated benchmark is observed to exhibit relatively higher power reduction where the excess current is utilized for driving longer wires decreasing buffer requirement. At an operating voltage of $V_{DD}$ = 0.4 V, the optimal NCFET is shown to yield *78%* iso-performance total power reduction compared to the baseline operating at $V_{DD}$ = 0.8 V.

NCFETs with enhanced drain currents are desirable for improving performance. But the negative capacitance effect abruptly increases both drain current and gate capacitance at low gate voltages. The effective delay is determined by the ratio of the gate capacitance and drain current ($t = Q/I$) at the operating voltage of interest. NCFETs exhibiting high drain current operate faster at low voltages. As voltage increases, the NCFETs with less abrupt transfer characteristics start providing lower delay due to low capacitance overhead. Certain high-performance NCFETs lose negative capacitance enhancement at higher gate voltages, leading to additional performance deterioration. Therefore, the ferroelectric parameters providing maximum drain current constitute the minimum delay region at extremely low voltage which gradually shifts towards NCFETs with lower drain current enhancement as voltage increases. Energy-delay-product (EDP) optimization is considered to collectively optimize both performance and power. Feasible NCFETs with low drain current provide the maximum power reduction leading to distinct high performance and low power NCFETs. Optimal EDP reduction is provided by a distinct subset of NCFETs between the above two. As voltage increases, both high-performance and optimal EDP regions shift towards low drain current NCFETs as they become faster. At an operating voltage of $V_{DD}$ = 0.4 V, the optimal NCFET is shown to yield more than a node improvement with *61%* total power reduction and *44%* performance improvement compared to the baseline operating at $V_{DD}$ = 0.8 V.

# CHAPTER 1
# INTRODUCTION

Computing applications continuously demand technology improvements to achieve higher performance and lower power consumption. High-performance computing solutions with a high power budget, require faster processing technologies whereas battery-powered mobile computing technologies require energy efficient low power technologies. Conventional Complementary Metal Oxide Semiconductor (CMOS) technology has been employing Dennard scaling based physical feature size reduction to improve power and performance in successive technology nodes. Alternative technologies are required as transistor scaling is approaching the critical limits of atomic dimensions. Further, CMOS technology is limited by Boltzmann tyranny limiting sub-threshold slope to a minimum of 60 mV/decade. Negative Capacitance Field Effect Transistor (NCFET) is a fast emerging alternative CMOS technology that offers tremendous power and performance benefits. NCFET requires minimal fabrication overhead and therefore, it is an attractive low power technology.

NCFET is a steep slope switching device which was first proposed in [1]. The negative capacitance induced electrostatic voltage amplification facilitates significantly increased on-current at low gate voltages with sub-threshold slopes below the Boltzmann limit of 60 mV/decade [2]. The low sub-threshold slope and enhanced on-current characteristics of NCFET enable ultra-low voltage device operation leading to significant power reduction. The NCFET enhanced drain current behavior can also be employed to aggressively minimize device delay and achieve a higher frequency of operation. Therefore, the NCFET device is capable of (i) providing the same drain current as the baseline FET at reduced voltage and (ii) providing enhanced drain current than baseline FET for the same gate voltage. Consequently, NCFET is a feasible technology solution to cater both high performance and low power computing applications.

## 1.1 Prior Art

There have been several works in the literature exploring various aspects of NCFET characteristics. Following is the review of existing relevant works and their contributions. The multi-fold power reduction facilitated by the enhanced on-current behavior of NCFET has been explored in [1, 3, 4, 5, 6, 7]. Negative Capacitance FinFET devices fabricated utilizing $HfZrO_2$ and silicon doped hafnia have been experimentally demonstrated to show low sub-threshold slopes in [8, 9] respectively attracting significant research interests into this new device technology. The effects of ferroelectric layer thickness on NCFET device hysteresis and annealing temperature on sub-threshold slope are also explored in [8]. The devices fabricated in [9] also reveal tremendous current improvement of 75% for NMOS and 165% for PMOS. Further, 101 stage FO3 inverter ring oscillators running at extremely high frequencies are also reported in [9].

In order to enable circuit design and analysis, NCFET device modeling has been discussed in several publications [5, 6, 10]. The effects of ferroelectric layer thickness on delay and ferroelectric properties on the negative capacitance of NCFET have also been analyzed in [6]. The theoretical intrinsic delay of doped $HfO_2$ is predicted to be $\approx 270$ fs in [11] which indicates that the ferroelectric layer switching speed is lower than typical high-performance FinFET transition time. The effect of ferroelectric properties on ferroelectric capacitance and NCFET characteristics is discussed in [4]. Further, a strategy to avoid hysteresis under process variations is also devised in [4]. Full-chip implementation flow and power benefit study at multiple design levels pertaining to various applications with a single NCFET have been reported in [7].

## 1.2 Contributions

The Negative Capacitance Field Effect Transistor (NCFET) characteristics depend on ferroelectric properties in addition to the baseline FET parameters. The NCFET device profile

including the desirable abrupt current enhancement and low sub-threshold slope characteristics are primarily determined by the ferroelectric parameters and operating voltage. The ferroelectric parameters influence the ferroelectric capacitance added to gate dielectric stack and the operating voltage determines the degree to which the negative capacitance affects device characteristics. Further, the ferroelectric parameters must be chosen properly to avoid unstable operation caused by hysteresis.

Ferroelectric parameters and associated operating voltages are exhaustively analyzed in this work. The power and performance characteristics of NCFET are studied independently to effectively utilize the negative capacitance and achieve maximum power reduction and performance improvements. The NCFET characteristics are explored at multiple design levels such as device, logic-gate, and full-chip for obtaining a holistic idea of NCFET behavior, facilitate root-cause analysis, and associate power-performance effects to ferroelectric properties.

The comprehensive multi-level analysis yields the following counter-intuitive design guidelines:

1. NCFETs with the lowest sub-threshold slopes do not provide maximum power reduction and may actually increase power consumption under certain conditions.

2. NCFETs with the highest drain current may not always provide maximum performance improvement and under certain conditions, NCFETs with the minimum drain current may provide higher performance improvement.

In the above guidelines, the appropriate optimal or adverse conditions for an NCFET are primarily determined by operating voltage.

NCFETs with different groups of ferroelectric parameters are found to provide maximum power/performance at different operating voltages. Similarly, each combination of ferroelectric parameters can be associated with an optimal operating voltage to obtain maximum power/performance. The following lists the maximum and worst NCFET power-

performance characteristics among $V_{DD}$ = 0.4 V experiments compared to baseline FET (baseFET) implementations operating at $V_{DD}$ = 0.8 V.

- Optimal NCFET provides a maximum of 78% power reduction.
- Adverse NCFET increases power consumption by a maximum of 37%.
- Optimal NCFET provides a maximum of 62% performance improvement.
- Adverse NCFET reduces frequency up to 35%.
- Optimal NCFET provides a maximum of 81% EDP reduction resulting in more than a node improvement.

The NCFET power and performance optimization discussed in this work are submitted to multiple conferences and journals for publication.

### 1.3 NCFET notation

In this work, a negative capacitance field effect transistor with a given ferroelectric property is represented as $NCFET_{e,p}$ which denotes an NCFET with coercive field, $E_C$ = e MV/cm and remnant polarization, $P_0$ = p μC/cm$^2$.

### 1.4 Organization

The remaining chapters are organized as follows. Chapter 2 explains the negative capacitance transistor. The experimental setup is outlined in Chapter 3. Chapter 4 explores the ferroelectric properties and associated impact on device and logic gate characteristics. Chapter 5 demonstrates the power and performance results of full-chip implementations at $V_{DD}$ = 0.4 V. Finally, Chapter 6 explores the effect of operating voltage on power and performance characteristics.

# CHAPTER 2

# NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTOR

In a negative capacitance field effect transistor, the gate dielectric stack includes a ferroelectric oxide layer acting as an insulator with negative capacitance coupled with an interfacial layer [1] as shown in Fig. 2.1. The ferroelectric negative capacitance layer leads to an electrostatic amplification of the gate voltage at the oxide-semiconductor interface leading to a less than 60 mV/decade sub-threshold slope and significant on-current enhancement.

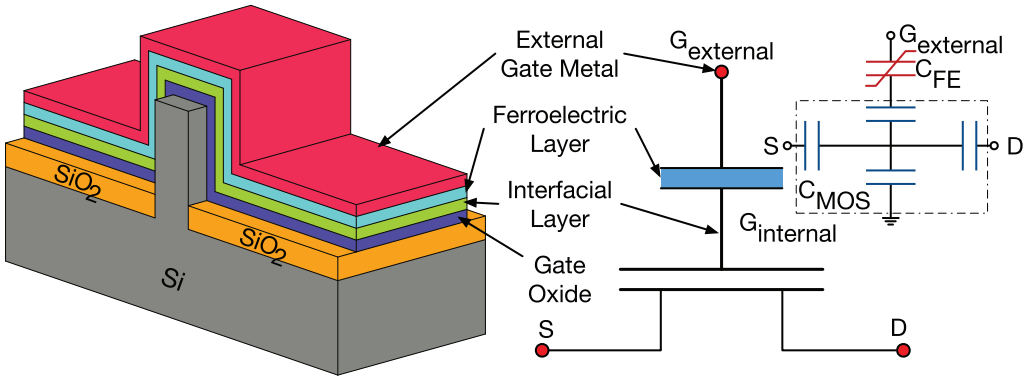



Figure 2.1: Device structure of a Negative Capacitance Field-Effect-Transistor (NCFET)

In this work, a 14 nm finFET is used as the baseline transistor (baseFET) and the NCFET shown in Fig. 2.1 includes an interfacial layer and a ferroelectric layer above the gate oxide. Inset of Fig. 2.1 shows the equivalent capacitance based circuit model of an NCFET. The equivalent capacitance of all the positive capacitors is modeled as $C_{MOS}$ and the NCFET effective gate capacitance can be determined by the following equation [3].

$$C_G = \frac{C_{FE}C_{MOS}}{C_{FE} + C_{MOS}} \tag{2.1}$$

Since $C_{FE}$ is negative, the effective gate capacitance ($C_G$) is greater than $C_{FE}$ and $C_{MOS}$ when $|C_{FE}| > C_{MOS}$. The gate capacitance enhancement leads to electrostatic voltage amplification that provides low sub-threshold slope and low voltage drain current enhance-

ment. NCFETs exhibit maximum capacitance enhancement leading to the lowest sub-threshold slope and maximum $I_{ON}$ without hysteresis under the condition $|C_{FE}| \approx C_{MOS}$ and $|C_{FE}| > C_{MOS}$ [4]. When $|C_{FE}| < C_{MOS}$ the effective gate capacitance becomes negative leading to hysteresis and unstable device operation.

Consider the following examples:

1. If $C_{FE} = -4$ fF and $C_{MOS} = 2$ fF, we get $C_G = 4$ fF resulting in 2X capacitance enhancement.

2. If $C_{FE} = -2.1$ fF and $C_{MOS} = 2$ fF, we get $C_G = 42$ fF resulting in 21X capacitance enhancement leading to tremendous drain current enhancement and significant sub-threshold slope reduction.

3. If $C_{FE} = -1.9$ fF and $C_{MOS} = 2$ fF, we get $C_G = -38$ fF resulting in negative effective gate capacitance and unstable device operation with hysteretic transfer characteristics.

The ferroelectric capacitance ($C_{FE}$) is determined by the ferroelectric parameters, primarily coercive field ($E_C$), remnant polarization ($P_0$), and ferroelectric layer thickness ($t_{FE}$). The impact of ferroelectric parameters on ferroelectric capacitance ($C_{FE}$) is given by the following equation from [4].

$$C_{FE} \approx -\frac{2}{3\sqrt{3}} \frac{P_0}{E_c t_{FE}} \tag{2.2}$$

The ferroelectric parameters must be selected carefully to avoid hysteresis. The device characteristics depend on $C_{FE}$ which is determined by ferroelectric parameters. Therefore, NCFET characteristics are determined by ferroelectric parameters such as coercive field ($E_C$), remnant polarization ($P_0$), and ferroelectric layer thickness ($t_{FE}$) in addition to base-FET parameters. Eqn. 2.2 shows that $C_{FE}$ decreases when remnant polarization decreases while all other ferroelectric parameters remain constant. Therefore, a decrease in remnant polarization increases the drain current and decreases sub-threshold slope.

Eqn. 2.2 also shows that ferroelectric capacitance is inversely proportional to coercive field and thickness of ferroelectric layer. Therefore, the drain current and sub-threshold slope improvement increase if $E_C$ or $t_{FE}$ increases while other parameters remain constant. If multiple parameters are varied, the resulting NCFET characteristics depend on the effective ferroelectric property variation. Since both coercive field and ferroelectric layer thickness influence capacitance in a similar way, it is sufficient to analyze the behavior of one of the parameters. In this work, the ferroelectric layer thickness is fixed to a constant value and the other two parameters (remnant polarization and coercive field) are analyzed exhaustively.

# CHAPTER 3

# DESIGN AND SIMULATION SETUP

This chapter describes the NCFET device, logic-gate, and full-chip level setup used to implement and perform multi-level analysis with various devices.

## 3.1 Device Model

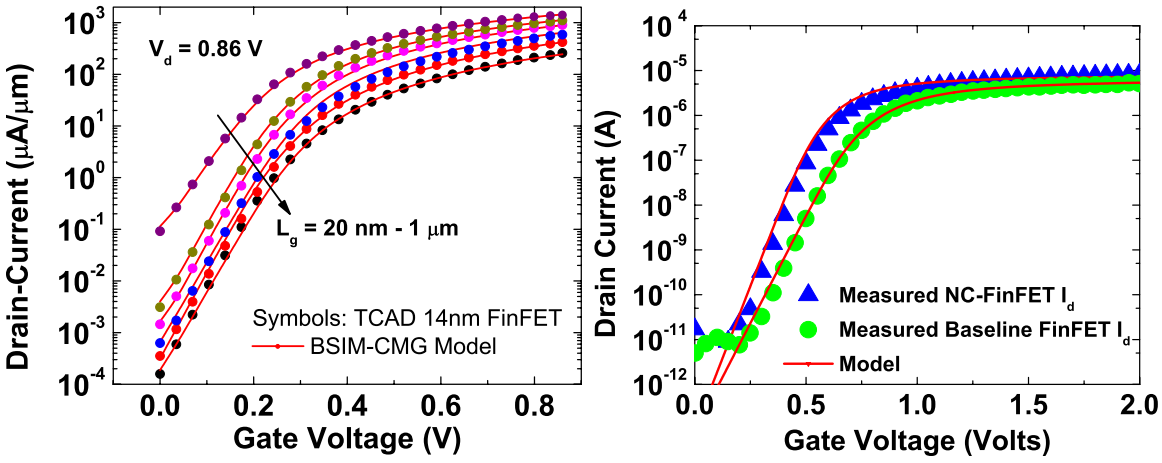



Figure 3.1: Model validation of BaseFET and NCFET devices

### 3.1.1 BaseFET Model

The BSIM-CMG 14nm finFET model developed in [12] is used as our baseline model (baseFET). BSIM-CMG incorporates accurate modeling for heterogeneous channel material devices and complex fin cross-sections. The baseFET is designed in accordance with ITRS 2015 [13] 14nm high-performance technology with the following parameters: fin height $H_{fin} = 42$ nm, fin thickness $T_{fin} = 5$ nm, gate length $L = 20$ nm and nominal $V_{DD} = 0.8$ V. Fig. 3.1 (a) shows the agreement between the BSIM-CMG model and TCAD for various gate lengths at $V_D$ = 0.86 V as depicted in [5].

### 3.1.2 NCFET Model

NCFET device modeling and analysis have been discussed in multiple works [5, 6, 10]. The ferroelectric layer is modeled by solving the three-dimensional electrostatics for baseFET self-consistently with single domain time-dependent Landau-Khalatnikov ($L - K$) model based on [5] and the fabrication data from [8]. The complete NCFET model is achieved by introducing the ferroelectric layer into the baseFET model and experimentally calibrating various parameters to match fabrication results. Fig. 3.1 (b) compares the NCFET and baseFET models with [8] measurements as depicted in [5]. The ferroelectric-layer response-time is predicted to be $\approx 270$ fs for doped Hafnium Oxide $HfO_2$ in [11], which is lower than typical 14nm device switching delay. In other words, the ferroelectric layer is predicted to be capable of switching at the speed necessary to satisfy 14nm device operation. The ferroelectric layer switching speed is further validated by the high frequency 101 stage FO3 inverter ring oscillators reported in [9]. The NCFET devices are modeled with constant off-current which is similar to baseFET, while the other characteristics depend on ferroelectric parameters in addition to the standard BSIM-CMG parameters.

This work improves the accuracy of NCFET device models in the following aspects:

1. Modern finFET technologies incorporate strain engineering that enhances hole carrier mobility leading to approximately equal PFET and NFET current capabilities [14]. Further, NCFET devices with 165% current enhancement for PFET are reported in [9]. Thus, both the baseFET and NCFET models are tuned to provide similar currents for NFET and PFET devices.

2. The source and drain terminals of a MOSFET (finFET) are dynamically determined based on the instantaneous voltage levels at either terminal. Therefore, the NCFET model is updated to allow swapped source-drain utilization which enables the design of logic gates using NCFET devices.

## 3.2 Standard Cell Library

Static CMOS standard cell library based digital logic design is prevalent in the industry. Nangate Open Cell Library (OCL) [14] which is designed based on freePDK15, is used to design the baseFET and NCFET standard cell libraries from logic gate netlists with parasitic information. Both freePDK15 and baseFET are developed in accordance with ITRS specifications [13] and therefore, it is suitable to design baseFET and NCFET standard cell libraries with OCL. In order to avoid extraneous deviations in the analysis of NCFET device performance, all the models are verified to comply with the following cell library design principles: (1) The Nangate Open Cell Library (OCL) [14] is designed based on hole carrier mobility enhancement leading to approximately equal PFET and NFET current capabilities. As discussed in the preceding section, the device models are tuned such that $I_{on,PFET} > 0.9I_{on,NFET}$ to satisfy OCL design assumption. (2) The usage of pass transistors and transmission gates require the ability to use source and drain terminals interchangeably as they are dynamically determined. The NCFET models are designed and validated to support such swapped usage.

NCFET cell library characteristics such as delay and power are explored for a single NCFET device in [7]. In this work, the power-performance characteristics of several NCFET devices with different ferroelectric parameter combinations are explored.

## 3.3 Benchmark Circuits

Two benchmark circuits AES-128 and LDPC are used to analyze the power and performance characteristics of NCFETs with various ferroelectric parameters and operating voltage combinations. AES-128 is a cell-dominated design which implements 128-bit advanced encryption standard (AES). The physical design of AES-128 is limited by gate placement with primarily local interconnects rendering it a cell-dominated design. On the other hand, LDPC is a wire-dominated Low-Density Parity-Check implementation. The

physical design of LDPC is limited by routing requirements triggered by an abundance of global interconnects rendering the design wire-dominant. Table 3.1 shows the benchmark iso-performance design constraints and the corresponding baseFET implementation results. AES-128 utilizes approximately twice the number of logic gates as LDPC whereas LDPC requires 10 metal layers for routing compared to the 6 metal layers needed for AES. Further, AES power consumption is dominated by internal power while LDPC power consumption is dominated by switching power.

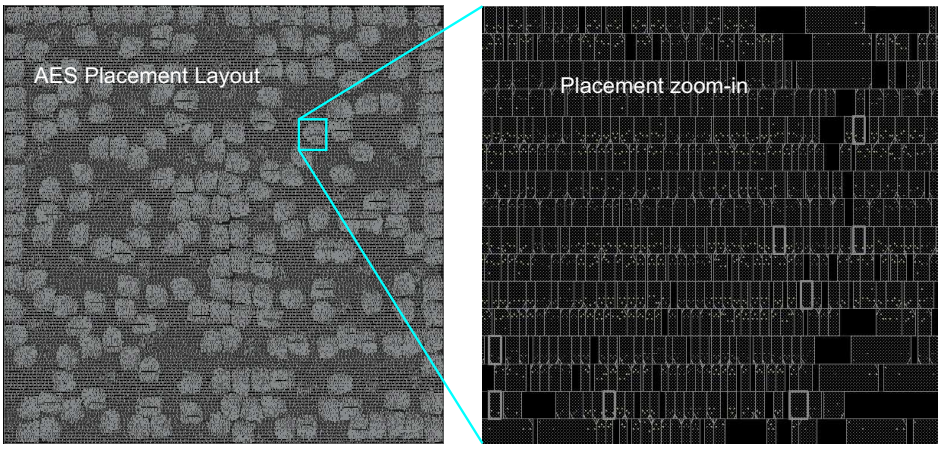
Table 3.1: Full-chip benchmark iso-performance statistics based on a 14nm PDK

| **Parameter** | **AES** | **LDPC** |
|---|---|---|
| Maximum Frequency (GHz) | 4 | 2.5 |
| Gate Count | 104,000 | 55,500 |
| Footprint ($\mu m^2$) | 53,000 | 28,000 |
| Wirelength (mm) | 820 | 1,000 |
| % Switching Power | 36 | 56 |
| % Internal Power | 62 | 43 |
| Metal Layer Count | 6 | 10 |

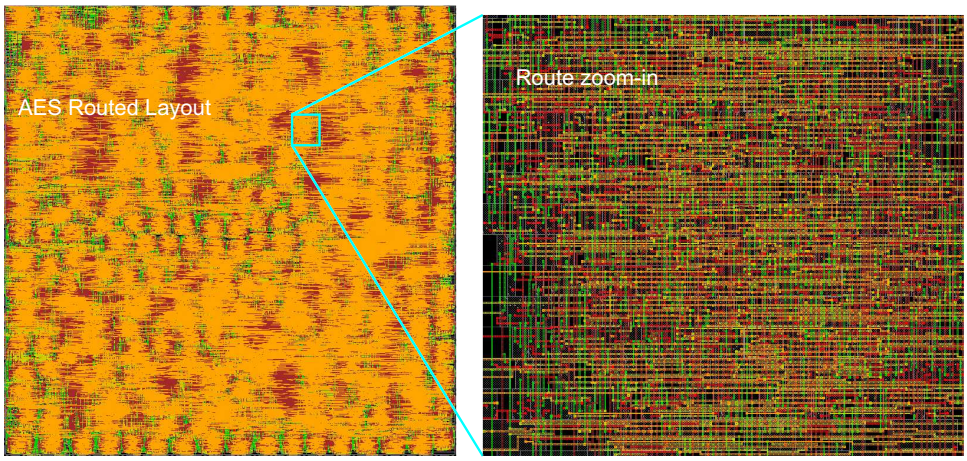
### 3.4 Implementation Flow

A single NCFET oriented full-chip implementation for designs of various sizes and limited effects of operating voltage variations for high performance and low power applications are discussed in [7]. A similar full-chip implementation flow is utilized in this work to study the effect of ferroelectric parameters and operating voltage.

The three ferroelectric parameters that primarily influence ferroelectric negative capacitance and ultimately the NCFET characteristics are given by Eqn. 2.2. The ferroelectric capacitance is affected in a similar way by the thickness of ferroelectric layer ($T_{FE}$) and coercive field ($E_C$) parameters. Therefore, the thickness of ferroelectric layer is fixed at a constant value of $T_{FE} = 5$ nm. An exhaustive set of NCFET devices with distinct $E_C$ and $P_0$ parameter combinations are analyzed to explore the power and performance behavior of NCFETs. $E_C - P_0$ are analyzed within the range corresponding to $HfO_2$ and its doped




(a) AES Placement




(b) AES Routed

Figure 3.2: Full-chip layout snapshots

variants as indicated in Table 4.1 based on ferroelectric property data from [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36]. The ferroelectric properties of NCFET devices fabricated in [8, 9] also lie within the same range.

The NCFET is first tested for feasible and stable device operation by examining the DC transfer characteristics for hysteresis (refer Sec. 4.2). Spice simulations also provide an insight into the optimal operating voltage for an NCFET with given ferroelectric properties. Synopsys SiliconSmart, a commercial characterization tool, is employed to generate the typical corner standard cell libraries using baseFET and various hysteresis-free NCFETs at different operating voltages.

The benchmark RTL designs are synthesized using Synopsys Design Compiler for each generated library. Iso-performance power reduction analysis needs all benchmarks to be implemented at the maximum performance achieved by baseFET (reference). Whereas the maximum performance analysis demands each implementation to meet the maximum possible frequency. Therefore, the power and performance exploration necessitate individual full-chip implementations.

Physical design further needs interconnect technology information for RC calculation. The capacitance tables and interconnect technology files are developed using parasitic information from [13, 14]. The OCL design environment provides the physical standard cell library view (LEF). The synthesized benchmark designs are then placed and routed with the above physical information using Cadence Innovus Implementation system. Fig. 3.2 shows the full-chip layout snapshots for AES implementation.

Finally, the timing and power of the implemented designs are analyzed using sign-off grade Synopsys PrimeTime tool. All the NCFET implementations that satisfy the required timing criteria are explored for iso-performance power analysis. In the case of performance analysis, each NCFET is studied at the maximum frequency it offers and therefore, all the non-hysteretic NCFETs are considered.

# CHAPTER 4

# FERROELECTRIC PROPERTY IMPACT ON NCFET CHARACTERISTICS

The ferroelectric properties of an NCFET determine the ferroelectric capacitance ($C_{FE}$) of the device which in turn influences the NCFET characteristics. The effect of ferroelectric parameters on NCFET characteristics and ultimately the full-chip power-performance characteristics are exhaustively studied in this thesis. Equation 2.2 indicates that coercive field ($E_C$), remnant polarization ($P_0$), and thickness of the ferroelectric layer ($t_{FE}$) are the primary parameters and specifies their influence on ferroelectric capacitance. In this section, the impact of ferroelectric properties on NCFET characteristics such as sub-threshold slope, drain current and gate capacitance are explored.

## 4.1 Range of Ferroelectric Parameters

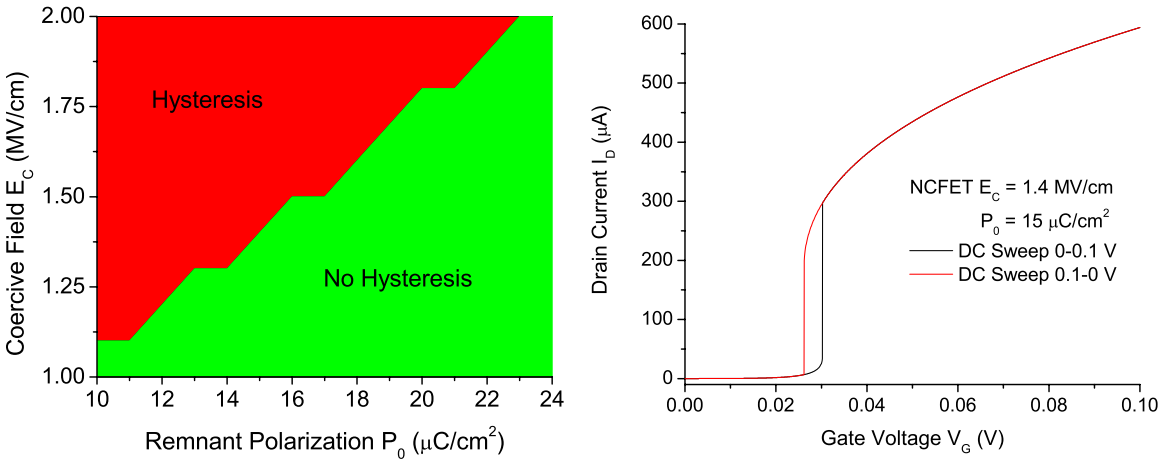
Ferroelectric capacitance is inversely proportional to both coercive field and ferroelectric layer thickness. Therefore, the thickness of the ferroelectric layer is fixed to $t_{FE}$ = 5 nm in accordance with the dimension of NCFET fabrication experiments in [8, 9]. The remaining two parameters coercive field and remnant polarization are studied between the ranges specified in Table 4.1 based on ferroelectric property data of $HfO_2$ and their doped variants in [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37].

Table 4.1: Range of Ferroelectric Parameters used to investigate NCFET characteristics

| **Parameter** | **Minimum** | **Maximum** |
|---|---|---|
| Coercive Field | 0.5 MV/cm | 2 MV/cm |
| Remnant Polarization | 10 μC/cm$^2$ | 40 μC/cm$^2$ |

Various NCFETs exhibiting an exhaustive combination of ferroelectric $E_C$ and $P_0$ parameter values are examined to assimilate NCFET behavior.

## 4.2 NCFET Hysteresis




(a) Hysteresis analysis (b) Hysteresis example

Figure 4.1: NCFET Hysteresis: (a) Ferroelectric parameter effect on NCFET drain current hysteresis. (b)Example showing NCFET with $E_C$ = 1.4 MV/cm and $P_0$ = 15 µC/cm$^2$ showing drain current hysteresis on forward and reverse DC sweep.

NCFETs exhibit unstable operation when $|C_{FE}| < C_{MOS}$ leading to negative gate capacitance. A conservative design approach to avoid hysteresis under process induced parameter variations is discussed in [4]. In this work, NCFETs with exhaustive combinations of coercive field and remnant polarization values from the considered range are analyzed to obtain the relationship between ferroelectric properties and hysteresis. Fig. 4.1 (a) shows the distribution of NCFET hysteresis for various $E_C$-$P_0$ combinations. $C_{FE}$ can be decreased by decreasing remnant polarization or increasing coercive field as shown in Eqn. 2.2. Therefore, as NCFET remnant polarization decreases the corresponding maximum coercive field to avoid hysteresis also decreases. Similarly, as NCFET coercive field increases the corresponding minimum remnant polarization increases. For each remnant polarization value, the transfer characteristics of NCFETs with various coercive fields are explored to find the maximum coercive field that avoids hysteresis and plotted in Fig. 4.1 (a). An example transfer characteristics with hysteresis is shown in Fig. 4.1 (b) for $NCFET_{1.4;15}$ ($E_C$ = 1.4 MV/cm, $P_0$ = 15 µC/cm$^2$). In this case, the drain current follows different paths for

forward DC sweep (from 0 to 0.1 V) and reverse DC sweep (from 0.1 to 0 V) with $V_{DD}$ = 0.4 V. For the considered remnant polarization range,

- NCFET with minimum remnant polarization, $P_0$ = 10 µC/cm$^2$ starts exhibiting hysteresis at $E_C$ = 1.1 MV/cm.
- The maximum coercive field for avoiding hysteresis gradually increases as NCFET remnant polarization increases.
- NCFETs with remnant polarization, $P_0 >= 25$ µC/cm$^2$ do not exhibit hysteresis for the entire range of $E_C$ in this study.

### 4.3 Ferroelectric parameter effect on NCFET Sub-threshold slope

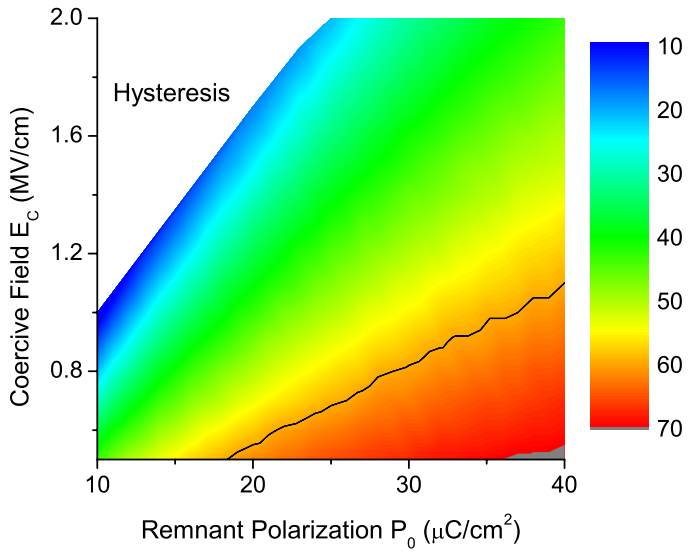



Figure 4.2: NCFET ferroelectric property effect on sub-threshold slope (mV/decade)

The sub-threshold slope distribution for all the NCFETs with remnant polarization and coercive field combinations that avoid hysteresis is shown in Fig 4.2. The lowest sub-threshold slope (7 mV/decade) is exhibited by NCFETs with minimum $|C_{FE}|$ whereas NCFET with maximum $|C_{FE}|$ exhibits the highest subthreshold slope (71 mV/decade). Therefore, the sub-threshold slope increases along the leading diagonal (from top-left to bottom-right).

NCFETs exhibiting the theoretical MOSFET minimum sub-threshold slope of 60 mV/decade are indicated by a black solid line in Fig. 4.2. Therefore, all the NCFETs below the demarcation exhibit sub-threshold slope above 60 mV/decade. Among NCFETs with low $|C_{FE}|$, the NCFETs with low remnant polarization exhibit more abrupt drain current enhancement and exhibit lower sub-threshold slopes. Therefore, the low sub-threshold slope values are concentrated at the low remnant polarization region and diverge as $P_0$ increases.

## 4.4 Ferroelectric parameter effect on NCFET transfer characteristics

The circuit power and performance behavior are primarily determined by the drain current and gate capacitance characteristics of the transistors used. In this section, the NCFET drain current and gate capacitance characteristics are exhaustively analyzed.

### 4.4.1 Effect of Remnant Polarization

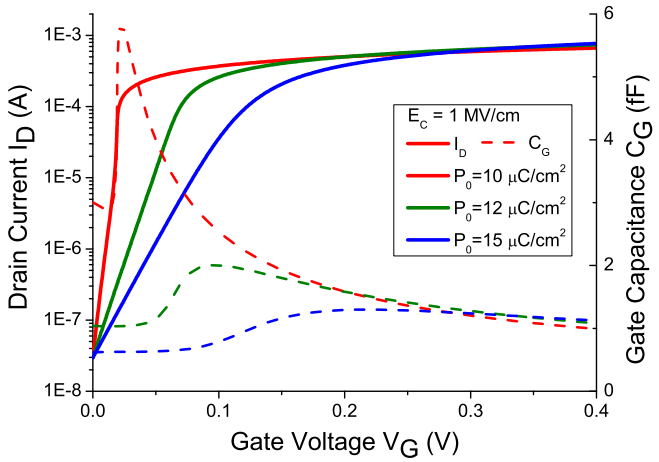



Figure 4.3: Transfer characteristics of NCFETs with various Remnant Polarization values

Fig. 4.3 shows the effect of remnant polarization on drain current and gate capacitance characteristics of NCFETs with constant coercive field $E_C$ = 1 MV/cm. Low remnant polarization NCFETs such as $NCFET_{1;10}$ exhibits enhanced drain current and gate capacitance at very low gate voltages. Therefore, such devices are characterized by very low threshold

voltages ($V_{th}$). An increase in remnant polarization leads to higher $|C_{FE}|$ which reduces the voltage amplification. Consequently, the threshold voltage increases as remnant polarization increases resulting in lower drain current and gate capacitance enhancement similar to $NCFET_{1;12}$ and $NCFET_{1;15}$.

As gate voltage increases, the drain current and gate capacitance enhancement slows down leading to drain current saturation and lower gate capacitance. When the gate voltage is increased further, the NCFET device exits negative capacitance mode with the ferroelectric layer exhibiting positive capacitance. The positive ferroelectric capacitance adversely affects NCFET performance based on Eqn. 2.1. This phenomenon is demonstrated by $NCFET_{1;10}$ in Fig. 4.3 where it exhibits abrupt drain current and gate capacitance surge at $V_G < 50$ mV. But when gate voltage increases to $V_G = 0.4$ V, the drain current and the gate capacitance of $NCFET_{1;10}$ decreases below that of the other NCFETs with higher remnant polarization. Therefore, decreasing NCFET remnant polarization enhances low voltage performance but deteriorates high voltage characteristics.

### 4.4.2 Effect of Coercive Field

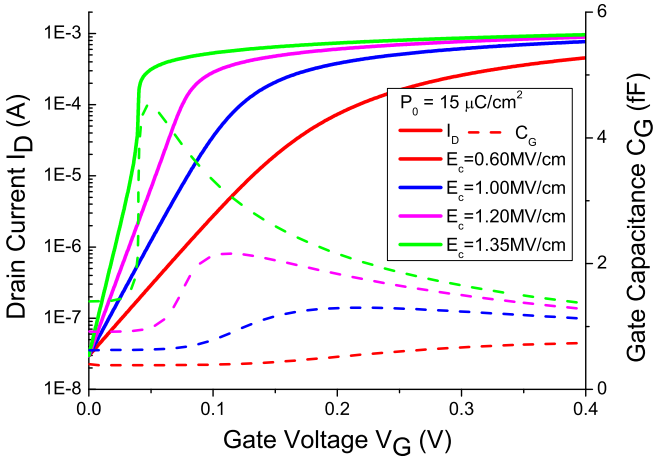



Figure 4.4: Transfer characteristics of NCFETs with various Coercive Field values

The effect of Coercive field on NCFET transfer characteristics is shown in Fig. 4.4 for devices with the same remnant polarization $P_0$ = 15 μC/cm$^2$. $NCFET_{1.35;15}$ with the highest

coercive field yields tremendous drain current enhancement with high gate capacitance. As coercive field decreases, the associated ferroelectric capacitance ($|C_{FE}|$) increases resulting in lower current and capacitance enhancement. High coercive field NCFETs exhibit low threshold voltages and as $E_C$ decreases the corresponding NCFET threshold voltage increases. Therefore, the other devices $NCFET_{1.2;15}$, $NCFET_{1;15}$ and $NCFET_{0.6;15}$ in Fig. 4.4 show gradually decreasing current and capacitance enhancement characteristics.

The drain current and gate capacitance enhancement decreases at higher gate voltages resulting in current saturation and a decline in capacitance. Despite exhibiting a low subthreshold slope of 50.5 mV/decade, the transfer characteristics of $NCFET_{0.6;15}$ increase gradually in contrast to the other NCFETs in Fig. 4.4. Therefore, the gate capacitance of $NCFET_{0.6;15}$ increases throughout the considered voltage range. One more interesting observation is that high coercive field $NCFET_{1.35;15}$ provides the highest drain current throughout the voltage range in Fig. 4.4. This indicates that higher coercive field primarily affects NCFET drain current enhancement but does not contribute as much to high voltage performance deterioration.

### 4.4.3 Combined Effect of Coercive Field and Remnant Polarization

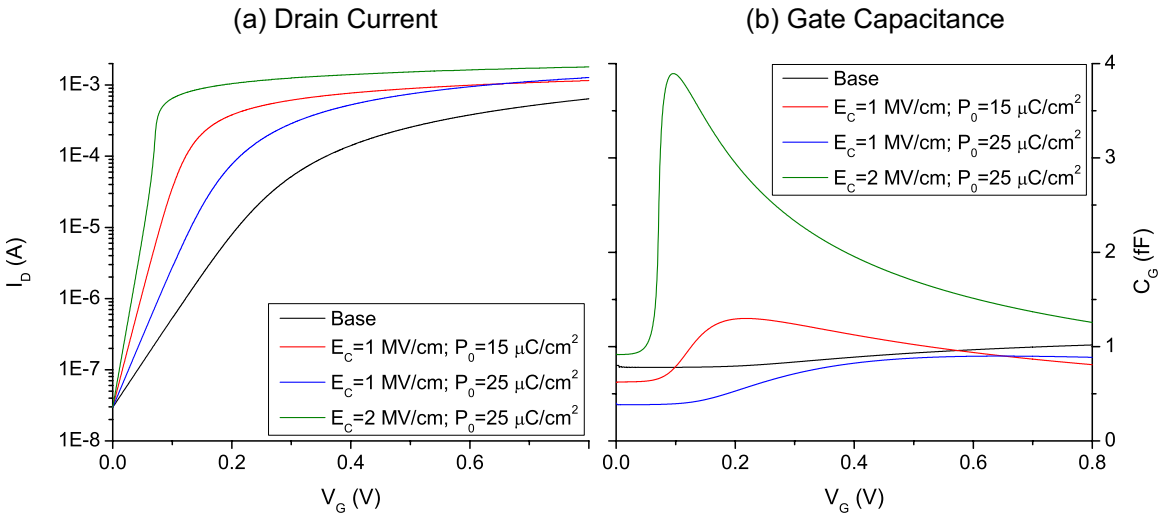



Figure 4.5: NCFET characteristics at $V_{DD}$ = 0.4 V

Fig. 4.5 compares the drain current and gate capacitance of NCFETs with that of baseFET at drain voltage $V_D$ = 0.4 V. Fig. 4.5 shows that (1) high coercive field $NCFET_{2;25}$ yields the highest drain current and (2) low remnant polarization $NCFET_{1;15}$ exhibits low threshold voltage but deteriorates performance at high gate voltages (3) High $|C_{FE}|$ NCFETs are characterized by non-abrupt drain and gate capacitance behavior as indicated by $NCFET_{1;25}$ and (4) All three NCFETs exhibit higher drain current and lower sub-threshold slopes than baseFET.

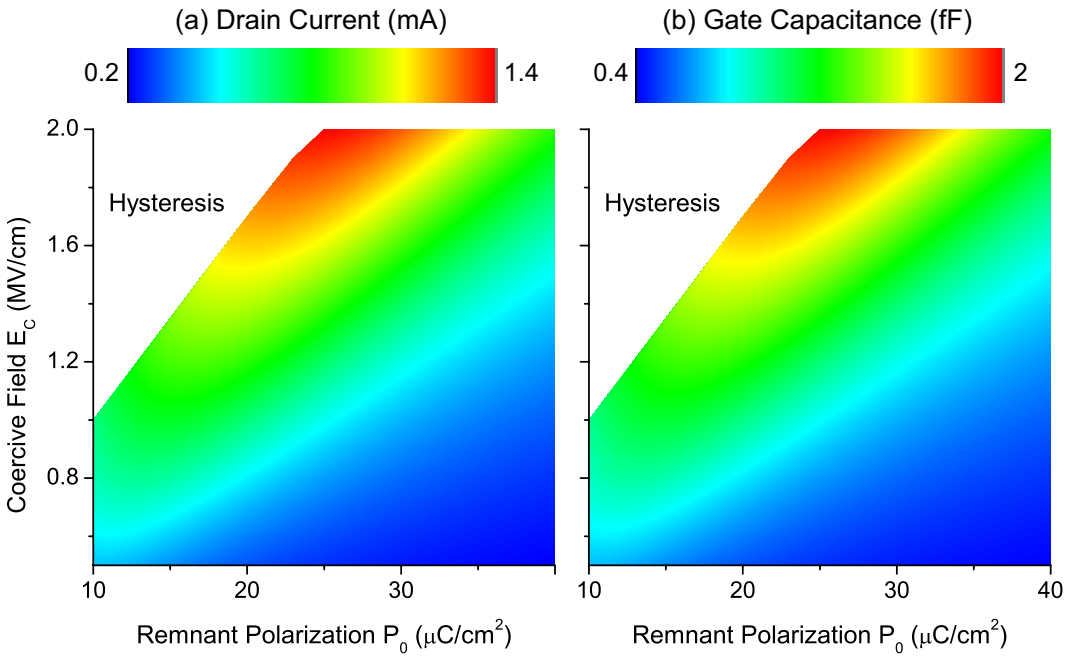



Figure 4.6: Distribution of NCFET current and capacitance at $V_{DD}$ = 0.4 V

From Fig. 4.3 and Fig. 4.4 it is evident that low remnant polarization NCFETs exhibit lower threshold voltages whereas high coercive field NCFETs provide a higher drain current enhancement. Further, Fig. 4.2 indicates that sub-threshold slope is primarily influenced by remnant polarization. The effective NCFET characteristics depend on the combination of coercive field and remnant polarization parameters:

- Low remnant polarization tremendously improves low voltage performance facilitating extremely low voltage operation. But at higher gate voltages the NCFET

loses ferroelectric negative capacitance enhancement and exhibits positive capacitance leading to performance deterioration.

- High coercive field tremendously improves drain current enhancement. The critical voltage at which the NCFET exits negative capacitance mode is primarily determined by remnant polarization. Thus, increasing coercive field does not lead to performance deterioration.

Fig. 4.6 shows the distribution of NCFET drain current and gate capacitance characteristics at $V_{DD}$ = 0.4 V for all the ferroelectric parameters combinations that avoid hysteresis (termed as viable ferroelectric parameter combinations in the below sections). In accordance with the above deductions:

- Vertical traversal of the distributions show that low $|C_{FE}|$ NCFETs with higher coercive field provide the highest drain current and gate capacitance.

- The receding behavior observed in the horizontal direction (from right to left) of drain and gate capacitance characteristics is caused by the low remnant polarization NCFETs exiting negative capacitance region before $V_{DD}$ = 0.4 V.

### 4.4.4 Notion of optimal delay

The negative capacitance induced electrostatic voltage amplification abruptly increases both drain current and gate capacitance of NCFETs. Therefore, the delay of NCFET is determined by the relative enhancement in gate capacitance and drain current. The ratio of accumulated gate charge to drain current at $V_{DD}$ = 0.4 V is plotted for the viable ferroelectric parameter combinations in Fig. 4.7. Irrespective of the dominant parameter contributing to the low ferroelectric capacitance ($E_C$ or $P_0$), the drain current enhancement slows down for high gate overdrive voltages. Fig. 4.7 indicates that the NCFETs with the highest drain current in Fig. 4.6 do not provide the minimum delay. Table 4.2 shows the drain current and estimated delay characteristics of two NCFETs where $NCFET_{2,25}$ with the

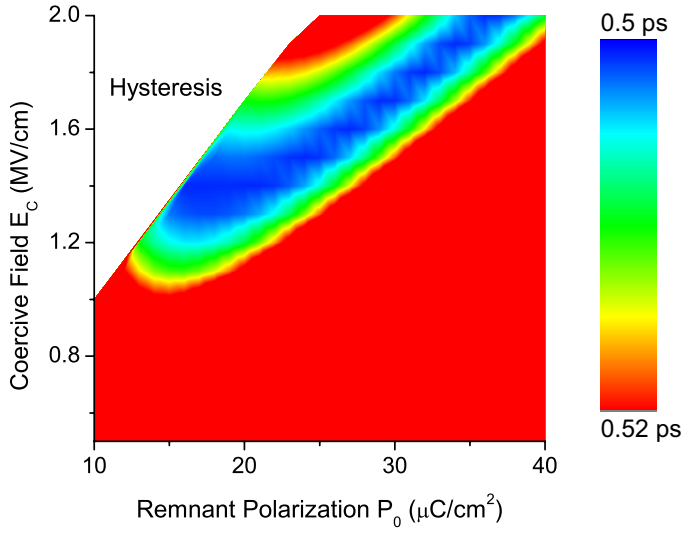



Figure 4.7: Minimum delay region at $V_{DD}$ = 0.4 V - Q/I(ps)

maximum drain current exhibits higher delay than minimum delay $NCFET_{1.5,25}$. Therefore, the distinct minimum delay region in Fig. 4.7 proposes the notion of optimal ferroelectric parameters that provide maximum performance.

Table 4.2: Maximum drain current and minimum delay at $V_{DD}$ = 0.4 V among NCFETs with remnant polarization $P_0$ = 25 μC/cm$^2$.

| NCFET Coercive Field MV/cm | Drain current (μA) | Delay estimation - Q/I (fs) |
|---|---|---|
| 2 | 1410 | 522 |
| 1.5 | 986 | 517 |

## 4.5 Ferroelectric Parameter Effect on Logic Gate Characteristics

The finFET based Nangate open cell library [14] is implemented using NCFET devices to explore the effect of ferroelectric negative capacitance on logic gate characteristics. In this work, the pin capacitance ($C_{PIN}$), short-circuit current ($I_{SC}$) and gate delay are studied to analyze the power-performance characteristics of NCFET circuits. The NCFET logic gate characteristics are studied at a constant operating voltage of $V_{DD}$ = 0.4 V. Further, the OCL is only implemented using a subset of the viable NCFETs that avoid hysteresis and other NCFETs exhibiting hysteresis are discarded. Three basic logic gates such as the inverter, 2-input Nand and D-flipflop (DFF) are considered for this analysis.

### 4.5.1 Pin Capacitance

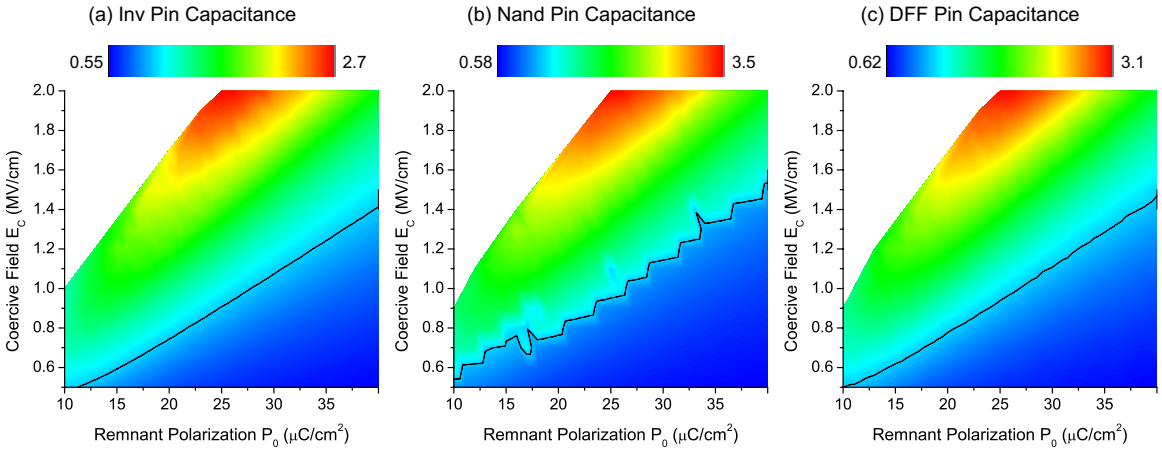



Figure 4.8: Ferroelectric parameter effect on pin capacitance of various NCFET logic gates operating at $V_{DD}$ = 0.4 V. The capacitances are normalized to that of the corresponding baseFET logic gate operating at $V_{DD}$ = 0.8 V.

Fig. 4.8 shows the ferroelectric parameter effect on input pin capacitance of the three basic gates. Input pin capacitance is the capacitance at a given input pin of the logic gate and is approximately the sum of all gate capacitances connected to the input pin. Therefore, input pin capacitance closely follows NCFET device gate capacitance distribution in Fig. 4.6. The performance deterioration instigated by low remnant polarization NCFETs exiting negative capacitance region for high gate voltages leads to the horizontal receding pattern observed in Fig. 4.8.

The capacitances in Fig. 4.8 are normalized to that of baseFET. The viable NCFET implementations of logic gates increase the pin capacitance up to 3.1 times that of baseFET. The black solid line indicates NCFETs that exhibit the same pin capacitance as baseFET and the NCFETs below this line exhibit lower capacitance than baseFET.

### 4.5.2 Short-Circuit Current

The effect of ferroelectric negative capacitance on inverter and Nand gate short-circuit current ($I_{SC}$) are shown in Fig. 4.9. The short-circuit current of a logic gate is primarily

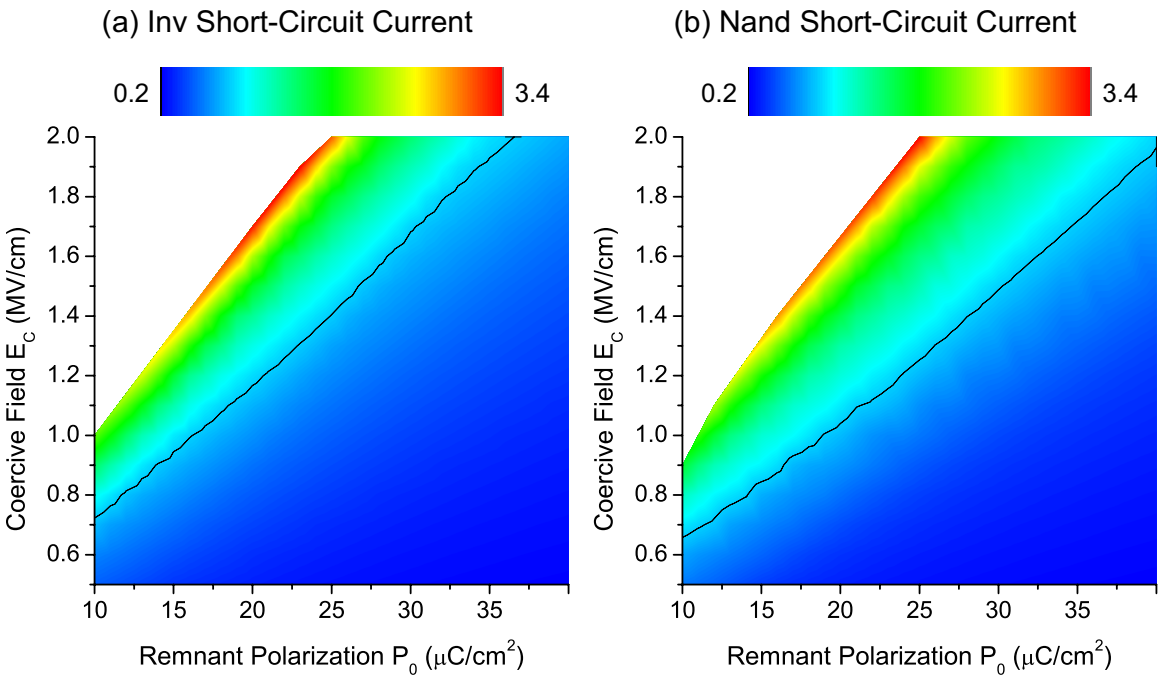



Figure 4.9: Ferroelectric parameter effect on short-circuit current of various logic gates operating at $V_{DD}$ = 0.4 V. The currents are normalized to that of the corresponding baseFET logic gate operating at $V_{DD}$ = 0.8 V.

determined by drain current capability and transition characteristics. The electrostatic voltage amplification induced drain current enhancement significantly increases short-circuit current. NCFETs with low ferroelectric capacitance especially the low remnant polarization NCFETs, exhibit very low threshold voltage owing to low-voltage current enhancement. Consequently, the period over which both NFET and PFET conduct increases which makes the transition difficult. Therefore, the high gate-overdrive voltage combined with enhanced drain current properties of NCFET significantly increase the transition window. The short-circuit current increases tremendously as a result of high drain current and transition window.

The voltage transfer characteristics and short-circuit current of three NCFET inverters are compared with that of baseFET inverter in Fig. 4.10.

- $NCFET_{1;25}$ with low gate-overdrive voltage exhibits sharp transition. But the short-circuit current is higher than baseFET due to drain current amplification.

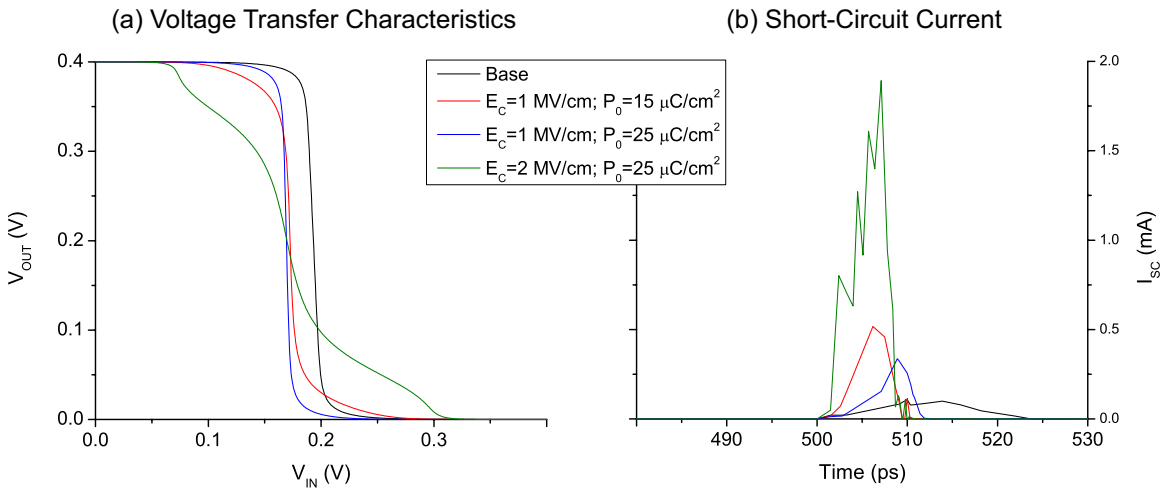



Figure 4.10: Comparison of baseFET and NCFET inverter characteristics at $V_{DD}$ = 0.4 V. (b) shows the short-circuit current consumed by a transition in the time interval (500 ps, 510 ps).

- $NCFET_{1;15}$ exhibits high gate-overdrive voltage owing to low $P_0$ leading to high transition window. This coupled with the high drain current increases short-circuit current.

- $NCFET_{2;25}$ provides the highest drain current enhancement and exhibits high gate-overdrive voltage. Fig. 4.10 (a) indicates that the transition is exacerbated by the enhanced drain current. The adverse drain current and transition window of $NCFET_{2;25}$ lead to tremendous short-circuit current consumption.

Fig. 4.9 indicates that the NCFETs with high drain current enhancement and low remnant polarization consume very high short-circuit current up to 3.4 times that of baseFET. The solid black line indicates the NCFET gates with $I_{SC}$ at $V_{DD}$ = 0.4 V equal to that of the corresponding baseFET gate at $V_{DD}$ = 0.8 V.

### 4.5.3 Delay

The logic gate delay is affected by the drain current capability and capacitance of underlying transistors. As the ferroelectric electrostatic voltage amplification increases both current and capacitance of NCFETs, the effective impact on delay is determined by the rel-

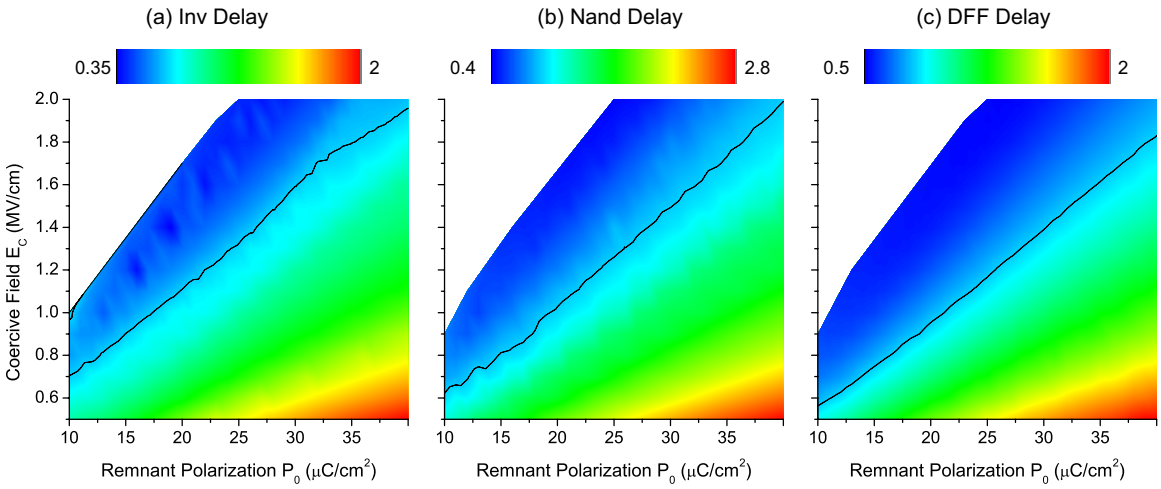



Figure 4.11: Ferroelectric parameter effect on NCFET logic gate delays at $V_{DD}$ = 0.4 V normalized to the corresponding baseFET gate delay at $V_{DD}$ = 0.8 V. D-Flipflop clock-to-Q delay is shown in (c).

ative enhancement between the two. Higher current enhancement decreases delay whereas higher capacitance increases delay.

Fig. 4.11 shows the delay distribution of three logic gates. The solid black line indicates NCFETs that exhibit the same gate delay as that of the corresponding baseFET at $V_{DD}$ = 0.8 V. The NCFET inverter yields the maximum speedup of 65% while Nand and D-flipflop exhibit 60% and 50% speedup respectively. High ferroelectric capacitance NCFETs increase the delay up to 180% compared to baseFET.

On closer analysis, the gate delay distributions contain regions of minimum delay towards the top left corner. The performance deterioration of low $|C_{FE}|$ NCFETs and performance improvement of marginally high $|C_{FE}|$ NCFETs lead to such minimum delay regions away from low $|C_{FE}|$ NCFETs. This behavior is similar to the minimum Q/I characteristics observed in Fig. 4.7 substantiating the notion of optimal ferroelectric parameters that minimize delay.

# CHAPTER 5

# ANALYSIS OF FULL-CHIP IMPLEMENTATION RESULTS AT $V_{DD}$ = 0.4 V

The AES and LDPC benchmarks are implemented using multiple NCFETs with viable ferroelectric parameters that avoid hysteresis. The operating voltage is fixed to a constant value of $V_{DD}$ = 0.4 V for all the analyses in this section. The baseline finFET device (baseFET) considered to evaluate the NCFET implementations in this work, is characterized with a nominal operating voltage of $V_{DD}$ = 0.8 V. As a reasonable comparison, all the 0.4 V NCFET implementations are compared with 0.8 V baseFET implementations to examine the ferroelectric property effect on full-chip power and performance. Further, the same floorplan area is used in the physical design of baseFET and NCFET based implementations for each benchmark.

## 5.1 Iso-performance full-chip power analysis

The ferroelectric negative capacitance induced electrostatic voltage amplification facilitates multi-fold power reduction in NCFET based implementation. In order to avoid extraneous deviations and examine the ferroelectric parameter effect on full-chip power:

- The maximum frequencies achieved in baseFET based AES and LDPC implementations are used as the target frequency for corresponding NCFET implementations.
- The target frequency for AES benchmark is 4 GHz whereas the target frequency for LDPC benchmark is 2.5 GHz.

Fig. 5.1 shows the effect of ferroelectric parameters on NCFET total, switching, and internal power reduction for both the benchmarks. The baseFET based AES and LDPC implementation constraints and power composition are listed in Table 3.1. The following characteristics are observed in the NCFET based benchmark implementations.

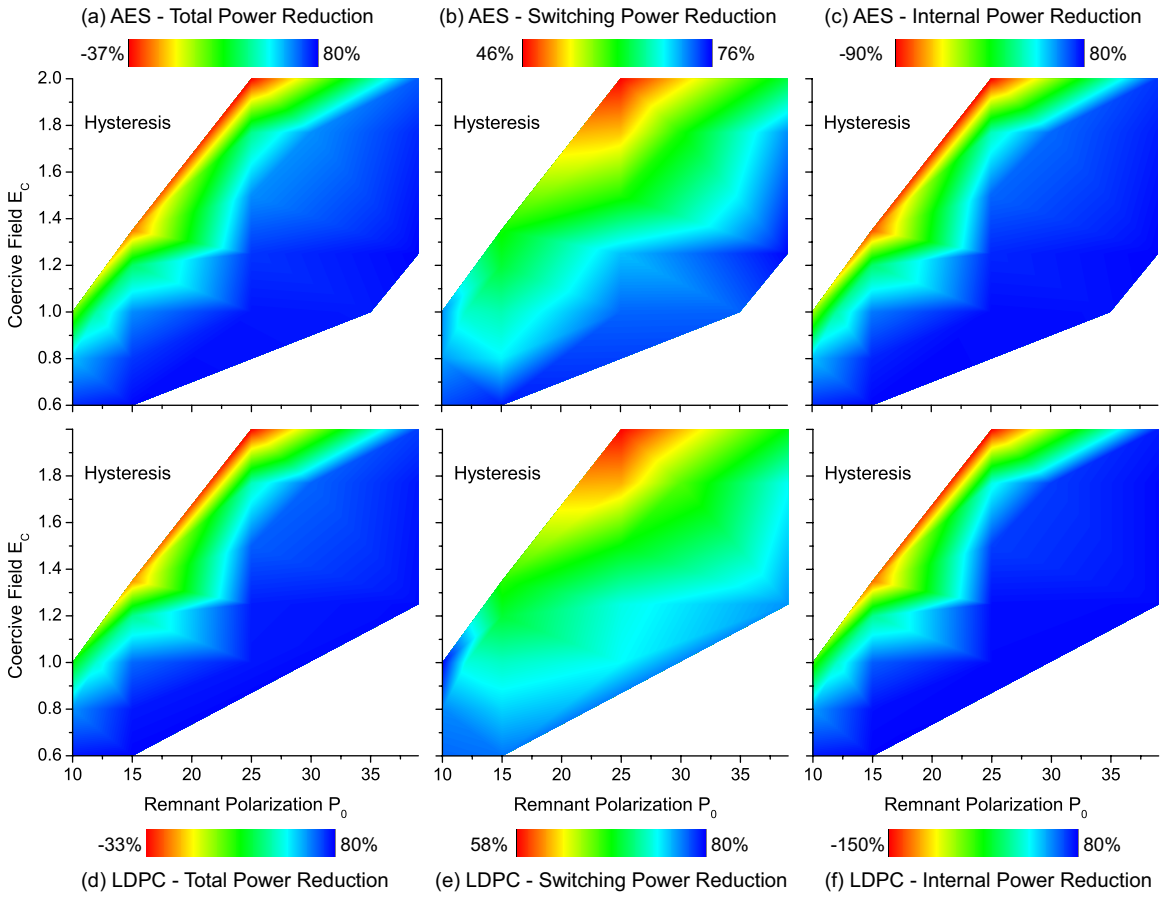



Figure 5.1: Effect of Ferroelectric Parameters on Full chip power at $V_{DD}$ = 0.4 V. (a)-(c) shows AES benchmark power distribution and (d)-(f) shows LDPC benchmark power distribution.

- The low $|C_{FE}|$ NCFETs which provide very high drain current at extremely low gate voltages exhibit lower delay than baseFET. Therefore, they easily satisfy the baseFET maximum frequency constraints for both the benchmarks.

- In the case of cell-dominated AES design, the NCFET basic implementation parameters such as gate count and wire-length are similar to that of baseFET owing to fixed floorplan area.

- Whereas in the case of wire-dominated LDPC, the NCFET drain current enhancement allows the logic gates to drive longer wires reducing the need for buffering. As a result, the standard cell area reduces up to 9% with high current NCFETs leading

to higher power reduction.

- The NCFET delay increases as $|C_{FE}|$ increases as depicted in Fig. 4.11. When NCFET delay increases beyond a critical value, the place and route tool starts compensating with larger gates and buffers. This increases the standard cell area and exacerbates power consumption.

- The high $|C_{FE}|$ NCFETs that do not provide sufficient performance and fail to meet the target baseFET maximum frequency are not considered for this analysis.

- Since the NCFETs are modeled with the same off-current as baseFET, the leakage current is similar for NCFETs operating at the same voltage. Hence both AES and LDPC implementations yield approximately 84% and 87% of leakage power reduction respectively owing to reduced operating voltage. The higher LDPC power reduction is caused by NCFET high-current induced gate count reduction.

### 5.1.1 Switching Power Characteristics

Switching power ($P_{SW}$) is the power consumed in switching the logic state of gate outputs. The capacitance connected to the output pin to be switched consists of interconnect wire capacitance and input pin capacitances of the driven logic gates. The wire capacitance remains approximately similar to that of baseFET implementation owing to fixed floorplan area. Hence the switching power distribution of both AES and LDPC in Fig. 5.1(b)(e) for constant $V_{DD}$ = 0.4 V closely matches that of gate capacitance and logic gate pin capacitance profiles shown in Fig. 4.6(b) and Fig. 4.8.

Reducing operating voltage leads to tremendous switching power reduction owing to the relation $P_{SW} \propto CV^2$ but the abrupt capacitance characteristic of NCFETs reduces the reduction in switching power. In this scenario, the 50% operating voltage reduction should yield an ideal switching power reduction of 75%. The low $|C_{FE}|$ NCFETs exhibit about 200% higher pin capacitance than baseFET as shown in Fig. 4.8. Therefore, the NCFET

switching power reduction is determined by the associated pin capacitance. Consider the following examples.

- Low $|C_{FE}|$ NCFET$_{2;25}$ implementation increases total pin capacitance by 150% and 130% for AES and LDPC benchmarks leading to minimum switching power reduction of 46% and 58% respectively.
- Implementation using NCFET$_{1.5;25}$ with relatively higher $|C_{FE}|$, increases total pin capacitance by 77% and 62% for AES and LDPC benchmarks providing a higher switching power reduction of 60% and 68% respectively.
- High $|C_{FE}|$ NCFET$_{0.6;15}$ actually decreases the total pin capacitance by 1.6% and 3.4% for AES and LDPC benchmark implementations resulting in a very high switching power reduction of 75.2% and 75.8% respectively. This is because of the high $|C_{FE}|$ NCFETs do not exhibit abrupt capacitance characteristics and exhibit gate capacitance below that of baseFET.
- Low remnant polarization NCFET$_{1;10}$ implementations of AES and LDPC provide 72% and 78% switching power reduction respectively. The extremely low remnant polarization causes such NCFETs to exit negative capacitance region and thereby reduce the gate capacitance.

The relatively higher switching power reduction observed for LDPC benchmark is due to the high-current induced gate-count reduction. Therefore, NCFET switching power consumption is primarily determined by pin capacitance, operating voltage, and design type.

### 5.1.2 Internal Power Characteristics

Internal power ($P_{INT}$) is the power dissipated within the logic gates. It is the sum of short-circuit power ($P_{SC}$) and internal node switching power ($P_{ISW}$). The internal node switching power exhibits the same characteristics as switching power ($P_{SW}$) due to the effect of ferroelectric parameters. Whereas short-circuit power is given by $P_{SC} = I_{SC} * V$.

The enhanced drain current and low threshold voltage induced tremendous short-circuit current exhibited by NCFET logic gates significantly increases short-circuit power consumption. Fig. 4.9 shows that NCFET implementations increase short-circuit current up to 240%. Further, the internal power distributions in Fig. 5.1(c)(f) are similar to the short-circuit current profile in Fig. 4.9 indicating that the internal power is dominated by short-circuit power characteristics.

Following are the internal power behavior of few NCFET implementations.

- Low $|C_{FE}|$ $\text{NCFET}_{2;25}$ with 200% higher $\text{I}_{\text{SC}}$, increases the internal power consumption by 88% and 154% for AES and LDPC benchmarks respectively. Since $\text{NCFET}_{2;25}$ does not increase switching power consumption, the internal power deterioration is due to associated tremendous short-circuit current and high transition window shown in Fig. 4.10.

- Similarly, low $|C_{FE}|$ $\text{NCFET}_{1.35;15}$ with 150% higher $\text{I}_{\text{SC}}$, increases internal power consumption by 75% and 130% for AES and LDPC benchmark implementations respectively.

- For $\text{NCFET}_{1;25}$ implementations, the internal power reduces by 78% and 79% for AES and LDPC respectively due to reduced pin capacitance, short-circuit current and transition window.

- $\text{NCFET}_{1;15}$ exhibits 60% internal power reduction for both the benchmarks due to higher transition window and pin capacitance.

- High $|C_{FE}|$ NCFETs exhibit low short-circuit current due to low gate-overdrive voltage and low drain current. Therefore, $\text{NCFET}_{0.6;15}$ provides the maximum internal power reduction of 81% owing to 60% lower short-circuit current.

Therefore, NCFET internal power consumption is primarily determined by short-circuit current, voltage transfer characteristics, operating voltage, and pin capacitance.

### 5.1.3 Total Power Characteristics

The total power consumption of the benchmark implementation is the weighted sum of individual power components such as switching power, internal power, and leakage power. At $V_{DD}$ = 0.4 V, all the NCFETs exhibit similar leakage power due to constant off current modeling. Further, Fig. 5.1 shows that the ferroelectric parameter effect on internal power is significantly higher than that of switching power for both the benchmarks. Therefore, the total power consumption is dominated by internal power and the total power reduction distribution under various ferroelectric parameter combinations is similar to that of internal power in Fig. 5.1. Following are the total power consumption characteristics of a few NCFETs.

- Low $|C_{FE}|$ $NCFET_{2;25}$ increases the total power consumption by 37% and 33% for AES and LDPC benchmarks respectively. The tremendous internal power consumption is compensated by reduced switching power resulting in marginally lower total power deterioration for $NCFET_{2;25}$.
- Similarly, low $|C_{FE}|$ $NCFET_{1.35;15}$ increases the total power consumption by 23% and 17% for AES and LDPC benchmarks respectively.
- $NCFET_{1.5;25}$ yields 62% and 68% total power reduction for AES and LDPC benchmarks respectively due to the similar reduction in internal power and switching power.
- For cell-dominated AES benchmark $NCFET_{1.25;39}$ provides the maximum total power reduction of 78.3%. It yields 77% LDPC total power reduction.
- $NCFET_{0.6;15}$ provides the maximum of 78% total power reduction for wire-dominated LDPC benchmark. It yields 78% total power reduction for AES benchmark.
- $NCFET_{1;10}$ with the lowest sub-threshold slope, provides 8% and 24% total power reduction for AES and LDPC benchmarks respectively.

## 5.2 Full-chip maximum frequency analysis

The drain current enhancement property of NCFET yields extremely low delay leading to significant frequency improvement compared to baseline FET. Further, the device and inverter delay analyses indicate the presence of minimum delay region with optimal ferroelectric parameters. In this section, the maximum performance achievable with viable NCFETs are explored. Both the benchmarks are implemented at the highest frequency that each NCFET based library satisfies.

Due to limited power budget for a given application, high-frequency operation under maximum power constraint is desirable. Therefore, energy-delay-product (EDP) is also considered to simultaneously maximize frequency enhancement and power reduction. Fig. 5.2 shows the maximum frequency, energy-delay product, and total power distribution for both the benchmarks using viable NCFET libraries at $V_{DD}$ = 0.4 V. Each of the distributions are observed to indicate optimal behavior at distinct ferroelectric parameter combinations.

### 5.2.1 Maximum Frequency Enhancement

The ferroelectric negative capacitance of NCFET increases both drain current and gate capacitance. The effective delay is determined by the relative variation of the two. The distributions of maximum frequency enhancement in Fig. 5.2 resembles the minimum delay distribution patterns in Fig. 4.7 and Fig. 4.11. Following observations are made from the maximum frequency distribution.

- Despite providing the maximum drain current, low $|C_{FE}|$ NCFETs provide marginally lower frequency enhancement due to higher capacitance. For example $NCFET_{2;25}$ with the highest drain current yields 27% and 41% frequency enhancement for AES and LDPC respectively.
- NCFETs with slightly higher $|C_{FE}|$ provide relatively enhanced drain current than capacitance and yield the maximum frequency improvement. $NCFET_{1.77;25}$ and $NCFET_{1.5;25}$

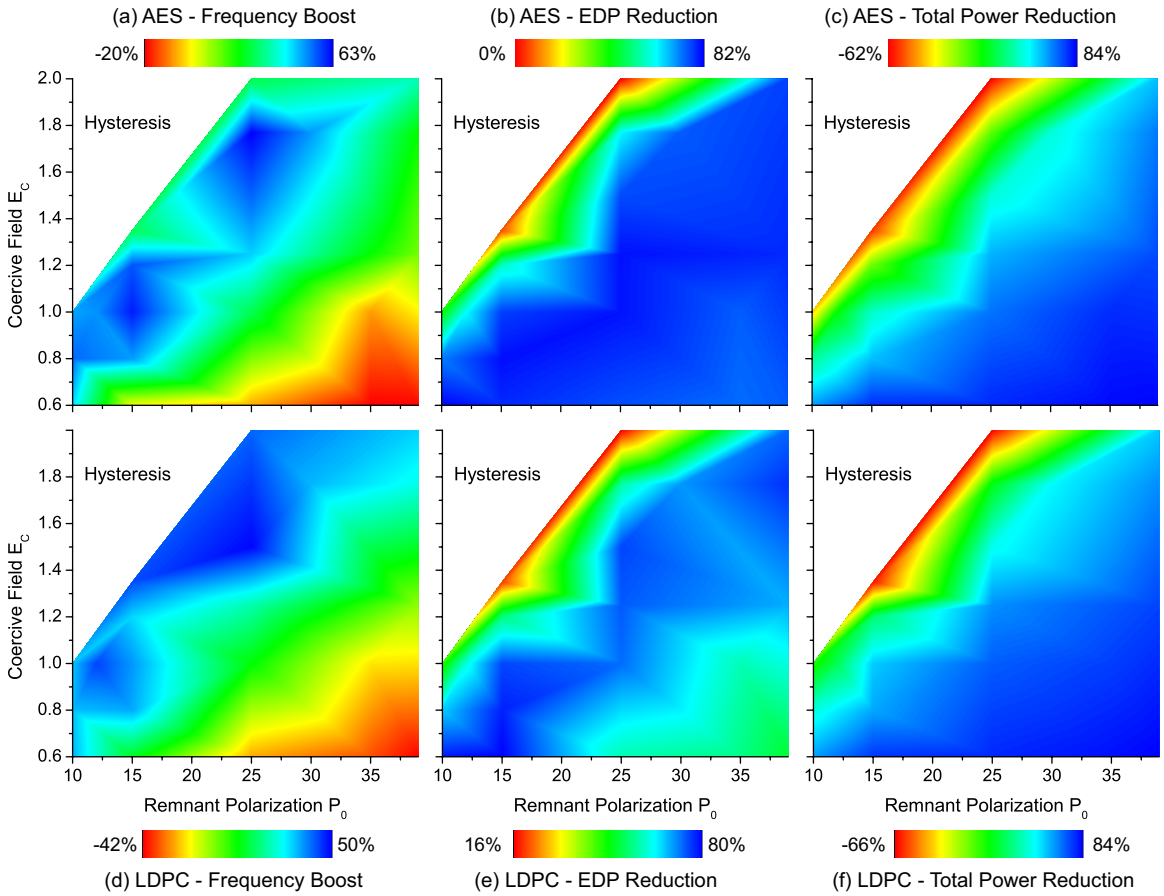



Figure 5.2: Effect of Ferroelectric parameters on NCFET Full-chip performance at $V_{DD}$ = 0.4 V. Frequency enhancement, EDP reduction, and power reduction are compared to that of the corresponding baseFET implementation at $V_{DD}$ = 0.8 V.

exhibit the maximum frequency enhancement of 62% and 50% for AES and LDPC benchmarks respectively.

- High $|C_{FE}|$ NCFETs do not provide sufficient drain current at $V_{DD}$ = 0.4 V leading to performance deterioration. For example, $NCFET_{0.6;39}$ implementations decrease the frequency of operation by 20% and 42% for AES and LDPC respectively.

Thus, full-chip maximum performance analysis confirms the existence of optimal ferroelectric parameters that provide minimum delay.

### 5.2.2 Total Power Reduction

The total power reduction characteristic resembles that of Fig. 5.1. But the range of power reduction has significantly increased due to the following effects.

- Very high $|C_{FE}|$ NCFETs are discarded from the iso-performance analysis as they do not satisfy frequency constraints. They are included in this analysis at their respective maximum frequencies and exhibit the maximum power reduction. Thus, the maximum power reduction marginally increases to 85%.

- As NCFET $|C_{FE}|$ decreases, the associated maximum frequency increases. Both the enhanced NCFET characteristics and increased frequency of operation exacerbate power consumption, thereby increasing the rate of power deterioration. For example, the total power reduction of $\text{NCFET}_{1.5;25}$ implementation reduces to $\approx 43\%$ under maximum frequency analysis compared to $\approx 68\%$ achieved in the iso-performance analysis.

- Similar to Fig. 5.1, very low $|C_{FE}|$ NCFETs exhibit maximum power consumption. For example, $\text{NCFET}_{2;25}$ implementation increases the total power consumption by $\approx 63\%$ for both the benchmarks.

- Among low $|C_{FE}|$ NCFETs, the devices with low remnant polarization exit negative capacitance operation region before 0.4 V leading to limited drain current improvement and low capacitance. Therefore, devices such as $\text{NCFET}_{1;10}$ consume 33% higher power for AES and 5% lower power for LDPC benchmarks.

### 5.2.3 Energy Delay Product Minimization

Fig. 5.2 shows that maximum frequency and minimum power are provided by NCFETs with ferroelectric parameters at either ends of the leading diagonal. Further, both frequency improvement and total power reduction exhibit wide ranges of variation. Therefore, the

following characteristics are observed for the EDP distribution which strives to maximize frequency and minimize power.

- Low $|C_{FE}|$ NCFET$_{2;25}$ exhibits high power consumption but also provides significant frequency enhancement leading to 0% and 16% EDP reduction for AES and LDPC respectively.

- NCFETs in and around the anti-diagonal (bottom-left to top-right) exhibit relatively lower drain current and capacitance enhancements. Therefore, such devices provide sufficient current with low capacitance at $V_{DD}$ = 0.4 V leading to maximum EDP reduction. For example, NCFET$_{0.8;15}$ yields 80% and 77% EDP reduction for AES and LDPC respectively.

- High $|C_{FE}|$ NCFETs actually decrease operating frequency leading to higher EDP. For example, NCFET$_{0.6;39}$ only yields 51% EDP reduction for LDPC benchmark.

Therefore, the NCFETs operating at $V_{DD}$ = 0.4 V can be classified into three distinct regions to optimize frequency, EDP, and power. In other words, as we move from top-left to bottom right, the NCFETs optimize frequency, EDP followed by power at the bottom right.

### 5.2.4 NCFET provides more than one node improvement

One node advancement is characterized by 30% performance improvement or 60% power reduction in conventional CMOS technologies. The maximum performance analysis reveals that NCFETs provide both *high-frequency enhancement and tremendous power reduction*. NCFET$_{0.6;10}$ in the optimum EDP region provides a remarkable 44% frequency improvement along with a tremendous 61% total power reduction for AES benchmark. For LDPC, NCFET$_{0.6;10}$ yields 34% frequency improvement coupled with 60% power reduction. Therefore, NCFETs provide more than one node improvement over baseFET by exhibiting remarkable frequency and power characteristics for a wide range of design types.

## 5.3 Inverter based Estimation

Based on the preceding multi-level analysis, it is observed that the power and performance effects of NCFET implementations are traced back to the underlying ferroelectric properties. Though complex circuits exhibit different characteristics than a simple inverter, the degree to which each property is influenced by the ferroelectric parameter is similar. Therefore, the ferroelectric parameter effect on full-chip power-performance characteristics can be estimated by analyzing a simple inverter behavior as shown below.

### 5.3.1 Power estimation

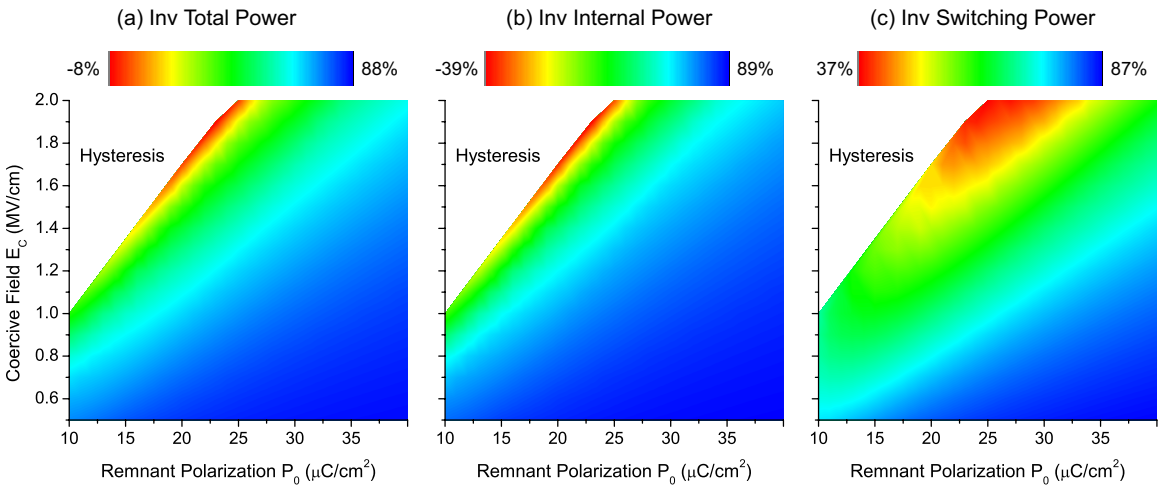
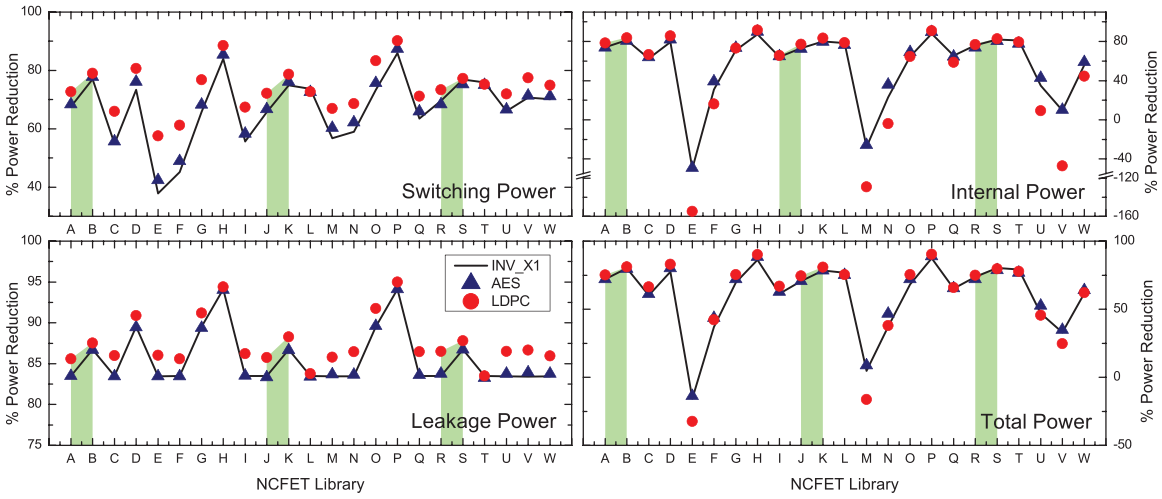



Figure 5.3: Estimation of power reduction with inverter ($V_{DD}$ = 0.4 V)

The pin capacitance and switching power characteristics of Fig. 4.8 and Fig. 5.1 show similar distribution. Similarly, the internal power distribution in Fig. 5.1 resembles that of Fig. 4.9. With this motivation, Fig. 5.3 shows the various power components estimated using inverter characteristics as follows.

- Switching power, $P_{SW,est} = C_{PIN}V_{DD}^2$
- Internal power, $P_{INT,est} = \alpha I_{SC}V_{DD} + \beta P_{SW,est}$
- Leakage power, $P_{LEAK,est} = I_{OFF}V_{DD}$




| | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O | P | Q | R | S | T | U | V | W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $P_0$ | 39 | 39 | 30 | 30 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 12 | 10 | 10 |
| $E_c$ | 1.77 | 1.77 | 1.77 | 1.77 | 2 | 1.77 | 1.77 | 1.77 | 1.5 | 1.25 | 1.25 | 1 | 1.35 | 1.2 | 1.2 | 1.2 | 1 | 0.8 | 0.8 | 0.6 | 1 | 1 | 0.8 |
| $V_{DD}$ | 0.4 | 0.35 | 0.4 | 0.3 | 0.4 | 0.4 | 0.3 | 0.2 | 0.4 | 0.4 | 0.35 | 0.4 | 0.4 | 0.4 | 0.3 | 0.2 | 0.4 | 0.4 | 0.35 | 0.4 | 0.4 | 0.4 | 0.4 |

Figure 5.4: Inverter vs. full-chip power comparison

Total power is estimated as a weighted sum of the power components based on design type. Fig. 5.4 shows that the inverter based power estimation effectively estimates the actual benchmark trend for each power component for multiple NCFET and operating voltages. INV_X1 power components are tuned to track AES behavior therefore, it does not predict LDPC gate count reduction and extreme power deterioration for the outliers accurately.

### 5.3.2 Performance estimation

The performance of NCFET based implementation at any design level only depends on the relative current and capacitance profiles. Consider the following comparison:

- High $|C_{FE}|$ NCFETs exhibit higher delay than baseFET in Fig. 4.11 and correspondingly fail to meet the baseFET maximum frequency in Fig. 5.1.
- A distinct minimum delay region exists in Fig. 4.11 leading to a corresponding maximum frequency region in Fig. 5.2.

Thus, inverter characteristics effectively estimate full-chip power and performance profiles of NCFETs with viable ferroelectric parameters.

## 5.4 NCFET Power Optimization

The drain current and gate capacitance of conventional CMOS devices do not exhibit abrupt characteristics and therefore, low sub-threshold slope and operating voltage are desired to minimize power consumption. But the enhanced NCFET characteristics lead to counter-intuitive power deterioration with low sub-threshold slope NCFETs. The following power optimization strategies are established by considering a combination of NCFET characteristics to exploit low voltage operation and achieve tremendous power reduction for a given iso-performance.

### 5.4.1 Preliminary Criteria

The following preliminary criteria attempt to exclude NCFETs that result in unstable operation, deteriorate power consumption, or insufficient performance.

1. Hysteresis free operation
2. Low gate delay $T_{d,NCFET} <= \gamma T_{d,BaseFET}$
3. $I_D$ enhancement throughout the voltage range

Among the preliminary criteria, (1) ensures stable device operation, (2) ensures that NCFET provides sufficient current to satisfy performance constraints and (3) ensures complete electrostatic voltage amplification to avoid performance deterioration. The multiplication factor $\gamma$ can be chosen according to the target design type. Therefore, the preliminary criteria assure that the target performance will be satisfied and power deterioration will be avoided by the corresponding NCFET implementation.

### 5.4.2 Optimal Selection

The NCFETs that meet the preliminary criteria should further satisfy the following criteria to maximize power reduction:

1. Low gate capacitance ($C_G$)

2. Low gate overdrive voltage ($V_{GS} - V_{TH}$)

3. Low Off-Current ($I_{D,OFF}$)

At constant $V_{DD}$, (1) decreases the switching power by minimizing capacitance overhead. Short-circuit power is minimized with (2) by decreasing transition window. (2) also discards NCFETs with very low sub-threshold slope as they exhibit low threshold voltage ($V_{TH}$). Leakage power consumption is minimized by (3) that selects NCFETs with low off-current.

### 5.4.3 Optimality Demonstration

The minimum operating voltage is primarily determined by the interconnect technology which is already a major limiting factor at smaller technology nodes [13]. Therefore, in order to demonstrate the optimality criteria let us consider a minimal 50 mV operating voltage reduction (from 0.4 V to 0.35 V) in accordance with ITRS 2015 [13]. Among NCFETs with various ferroelectric parameters listed in Fig. 5.4, three NCFETs are selected based on the above criteria. The transfer characteristics of the three NCFETs are shown in Fig. 5.5 and the corresponding inverter characteristics are listed in Table 5.1.

Table 5.1: Optimal NCFET INV characteristics

| **Device** | $\mathbf{C_{PIN}}$ **(fF)** | $\mathbf{T_d}$ **(ps)** | $\mathbf{I_{SC}}$ **(µA)** | $\mathbf{I_{OFF}}$ **(nA)** |
|---|---|---|---|---|
| $NCFET_{1.77;39}$ | 2.14 | 1.98 | 46.64 | 29.6 |
| $NCFET_{1.25;25}$ | 2.34 | 1.95 | 49.64 | 29.6 |
| $NCFET_{0.80;15}$ | 2.15 | 2.06 | 44.64 | 29.6 |
| BaseFET | 1.78 | 2.19 | 125.18 | 56.5 |

The selected NCFETs satisfy the preliminary criteria as (1) the transfer characteristics are free of hysteresis (2) they exhibit lower delay than baseFET and the transfer characteristics indicate continuous current and capacitance enhancement. However, $NCFET_{0.8;15}$

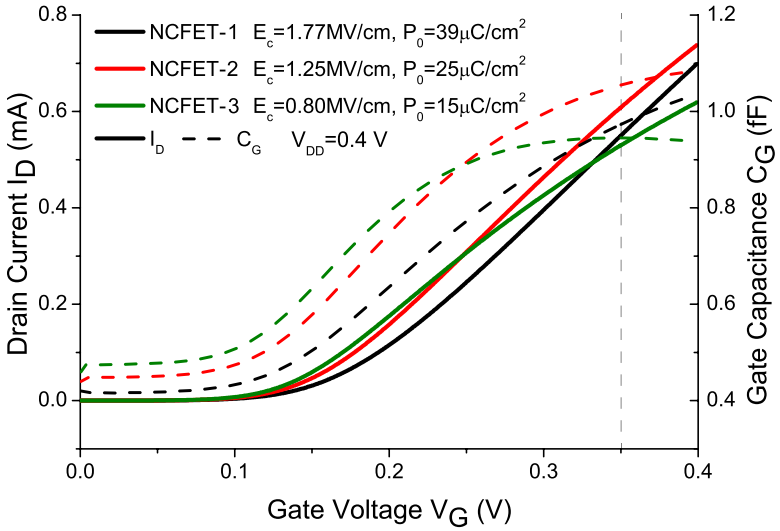



Figure 5.5: Transfer characteristics of NCFETs selected for optimality demonstration at $V_{DD}$ = 0.35 V.

with the lowest sub-threshold slope and remnant polarization has initiated exit from negative capacitance region indicated by the lowest drain current at $V_{DD}$ = 0.35 V. The selected NCFETs belong to the maximum power reduction region observed in Fig. 5.3.

The power reduction achieved using the selected NCFETs are highlighted in Fig. 5.4 and provide $\approx 25\%$ additional power reduction in each component compared to the corresponding NCFET at $V_{DD}$ = 0.4 V. Maximum total power reduction of 81% is achieved by $NCFET_{1.77;39}$ that best satisfies the optimization criteria with low capacitance and short-circuit current. $NCFET_{1.25;25}$ yields 79.6% and 81.5% power reduction for AES and LDPC respectively. The additional reduction in wire-dominated LDPC is due to high-current induced gate-count reduction. Whereas $NCFET_{0.8;15}$ with the lowest sub-threshold slope and short-circuit current exhibits 79.5% and 80.4% total power reduction for AES and LDPC respectively. Therefore, all the NCFETs selected through the optimization criteria provide tremendous power reduction subject to considered NCFETs and operating voltage. Further, it is observed that a small decline in the negative capacitance enhancement leads to apparent power deterioration.

# CHAPTER 6

# EFFECT OF OPERATING VOLTAGE

At $V_{DD}$ = 0.4 V, tremendous total power reduction, frequency enhancement, and EDP minimization are demonstrated in the preceding analysis using NCFETs with appropriate optimal ferroelectric parameters. Now, let us explore the impact of operating voltage variation on NCFET power-performance characteristics.

## 6.1 Sub-threshold slope analysis

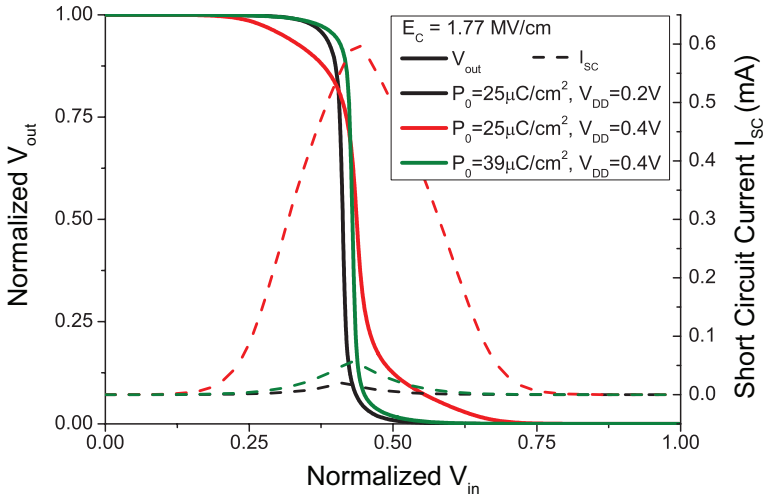



Figure 6.1: Inverter transfer characteristics

The gargantuan total power consumption observed in very low $|C_{FE}|$ NCFETs is due to associated enormous short-circuit current. This is caused by the high drain current and gate-overdrive voltage exhibited by such NCFETs. High drain current characteristic is desirable for improving performance as it results in lower delay. On the other hand, high gate-overdrive voltage has little contribution to performance enhancement but significantly increases power consumption. Due to the abrupt drain current enhancement, such NCFETs are capable of operating at extremely low voltages where they provide sufficient

drain current with low gate-overdrive voltage leading to substantially reduced short-circuit current. Consider the examples shown in Fig. 6.1, low $|C_{FE}|$ $NCFET_{1.77;25}$ based inverter consumes tremendous short-circuit current at $V_{DD}$ = 0.4 V compared to that designed using $NCFET_{1.77;39}$. As a result, the $NCFET_{1.77;25}$ implementations provide very low iso-performance internal power reduction of 39% and 16% for AES and LDPC respectively which is even lower than the expected reduction for 50% voltage reduction. At $V_{DD}$ = 0.2 V, $NCFET_{1.77;25}$ satisfies iso-performance timing constraints and significantly increases the internal power reduction to 90% and 92% for AES and LDPC respectively due to the sharp transition and very low short-circuit current shown in Fig. 6.1. Similar behavior is observed for $NCFET_{2;25}$ where internal power reduction increases from -123% and -204% to 73% and 78% for AES and LDPC respectively as $V_{DD}$ is reduced from 0.4 V to 0.2 V.

This results in an optimal NCFET usage guideline: each NCFET is characterized with an optimum operating voltage at which it exhibits maximum performance or minimum power consumption. Although low $|C_{FE}|$ NCFETs are capable of operating at extremely low voltages yielding tremendous power reduction, the minimum operating voltage for a given node is determined by the power distribution network limitations of the interconnect technology. The current and projected interconnect capabilities are outlined in [13]. Further, $NCFET_{2;25}$ with lower sub-threshold slope exhibits higher power consumption than $NCFET_{1.77;25}$ indicating that reducing sub-threshold slope leads to power deterioration due to higher drain current.

## 6.2 Inverter Power-Performance Exploration

In order to explore the effect of operating voltage variation on NCFET power and performance characteristics, let us consider NCFET inverter behavior. It is shown that the basic inverter characteristics effectively estimates Full-Chip power-performance characteristics in Section 5.3. Fig. 6.2 shows the normalized inverter power distribution at various operating voltages. The power calculations are done similar to Section 5.3.1.

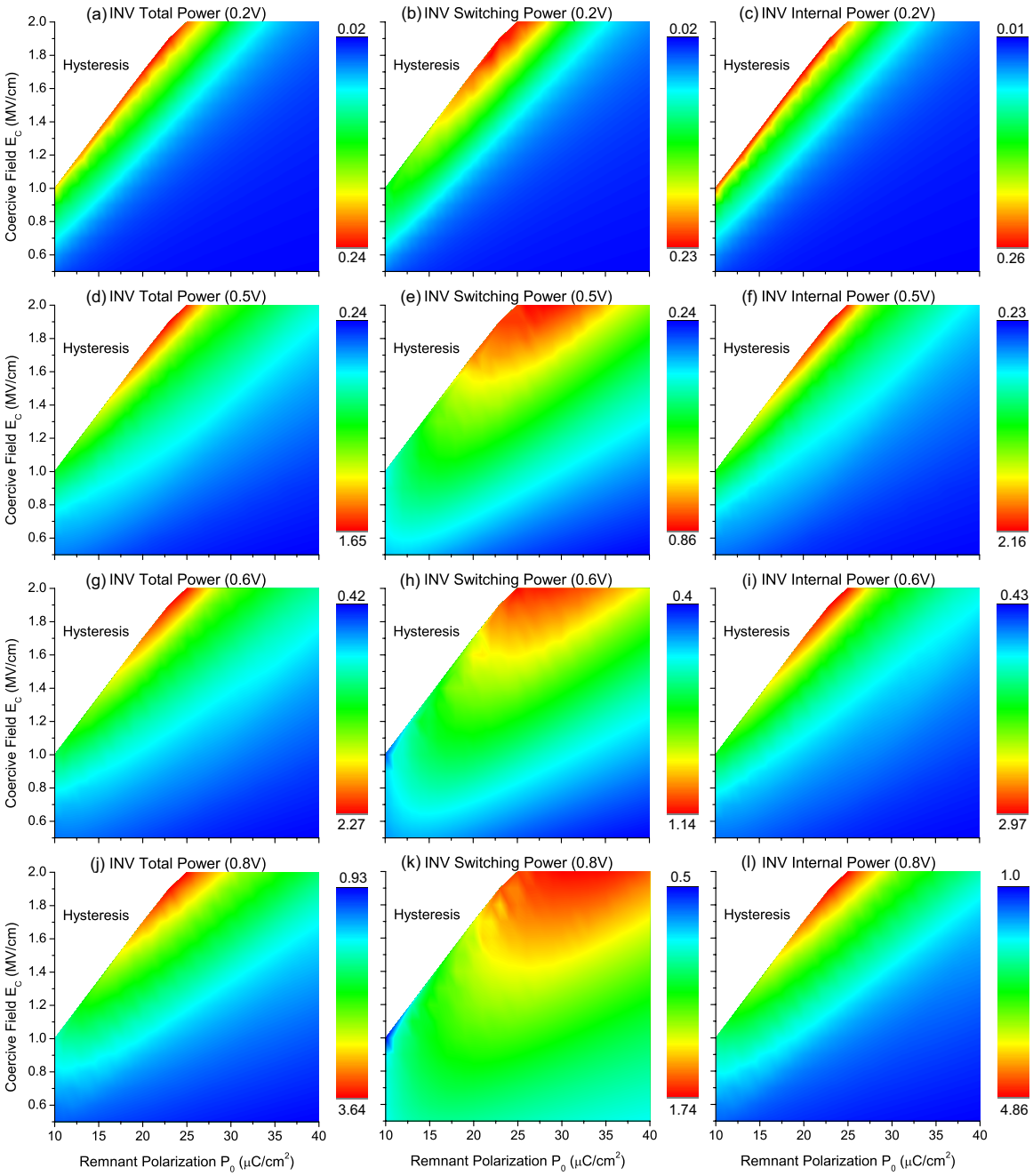



Figure 6.2: Impact of Vdd variation on NCFET inverter power characteristics. The NCFET inverter power consumption is normalized to that of baseFET operating at $V_{DD}$ = 0.8 V.

The switching power consumption distribution in Fig. 6.2 (b)(e)(h)(k) provides the following observations.

- Low $|C_{FE}|$ NCFETs consume high switching power due to higher gate capacitance and the power consumption reduces as NCFET $|C_{FE}|$ increases.

- All the NCFETs exhibit negative capacitance induced drain current and gate capacitance enhancement at $V_{DD}$ = 0.2 V. Therefore, the switching power increases as we move from top-left to bottom-right in the leading diagonal.

- As $V_{DD}$ increases, NCFETs with very low remnant polarization exit negative capacitance region leading to low gate capacitance. This causes the horizontal receding pattern observed at high $V_{DD}$. For a fixed coercive field, switching power increases as $P_0$ decreases up to a critical value. For $P_0$ values lower than the critical value, the switching power decreases due to low gate capacitance. Therefore, as $V_{DD}$ increases, the high switching power consumption region tilts horizontally towards the right.

- Whereas, the other NCFETs exhibiting negative capacitance continue to increase switching power consumption as $V_{DD}$ increases.

- An extreme case of the gate capacitance reduction for low remnant polarization NCFETs is observed at high $V_{DD}$ = 0.8 V where $NCFET_{1;10}$ exhibits the minimum inverter switching power.

As $V_{DD}$ increases the consumption of each power component increases but the magnitude of variation in internal power is much greater than switching power. Fig. 6.2 indicates that all power components exhibit similar consumption at $V_{DD}$ = 0.2V whereas at $V_{DD}$ = 0.8 V the internal power deterioration is 5 times that of switching power. Further, all NCFETs exhibit similar leakage power characteristics due to constant off-current modeling. Therefore, the total power distribution closely follows internal power characteristics. The internal power and total power distributions exhibit the following characteristics.

- Low $|C_{FE}|$ NCFETs exhibit high drain current leading to high power consumption. As NCFET $|C_{FE}|$ increases the sub-threshold slope increases and drain current decreases leading to lower power consumption.

- As $V_{DD}$ increases, the internal power deterioration increases drastically owing to abrupt transfer characteristics induced tremendous short-circuit current.
- The total power deterioration is lower than that of internal power due to low switching power deterioration.
- The loss of negative capacitance based enhancement in low remnant polarization NCFETs causes the maximum internal and total power regions to shrink along the anti-diagonal.
- High $|C_{FE}|$ NCFETs at the bottom-right corner exhibits minimum power consumption at all operating voltages.

Therefore, the non-abrupt drain current and gate capacitance characteristics of high $|C_{FE}|$ NCFETs provide the maximum power reduction at all the considered voltages.

Fig. 6.3 shows the distribution of inverter delay at operating voltages between 0.2 V and 0.8 V. An interesting phenomenon is observed in inverter delay characteristics, each operating voltage contains a distinct minimum delay region of NCFETs with optimal ferroelectric parameters.

- At $V_{DD}$ = 0.2 V, low $|C_{FE}|$ NCFETs provide high drain current leading to a maximum of 60% delay reduction whereas high $|C_{FE}|$ NCFETs exhibit orders of magnitude higher delay.
- As $V_{DD}$ increases, the relative enhancement in drain current is lower than that of gate capacitance for low $|C_{FE}|$ NCFETs. Further, NCFETs with slightly higher $|C_{FE}|$ that exhibit less abrupt current and capacitance characteristics exhibit lower delay. As a result, the minimum delay region gradually shifts from top-left to bottom-right with the increase in $V_{DD}$.
- NCFETs with very low remnant polarization exhibit high delay at $V_{DD}$ = 0.8 V owing to the loss of negative capacitance enhancement. Meanwhile high $|C_{FE}|$ NCFETs ex-

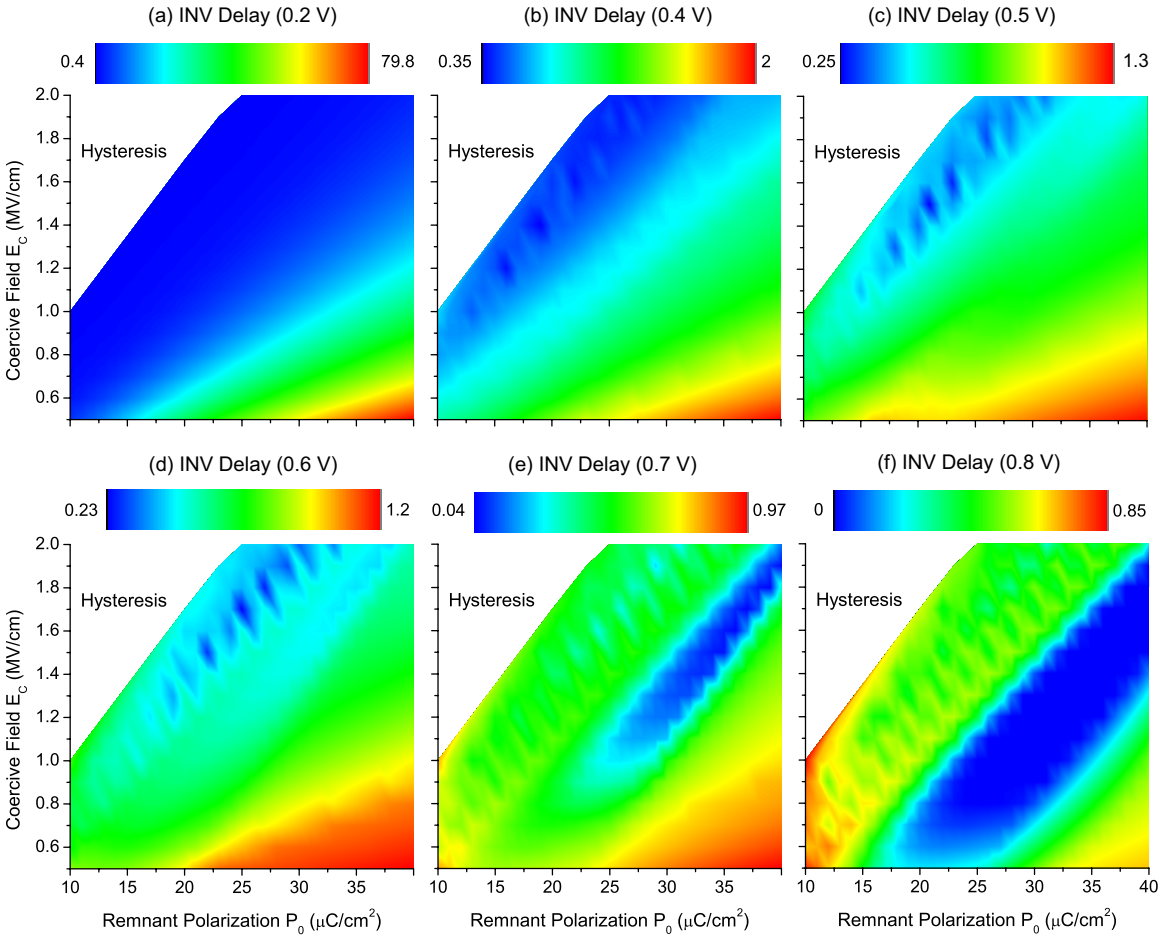



Figure 6.3: Impact of Vdd variation on NCFET inverter delay. The NCFET inverter delays are normalized to baseFET inverter delay operating at $V_{DD}$ = 0.8 V.

hibit lower delay as the non-abrupt transfer characteristics provide sufficient current at $V_{DD}$ = 0.8 V.

The following conclusions are drawn based on the inverter power-performance analysis.

1. Maximum performance enhancement and power reduction can be achieved by using NCFETs with optimal ferroelectric parameters that minimize delay and power respectively at the desired operating voltage.

2. Maximum power reduction can be achieved using NCFET with given ferroelectric parameters by operating at optimal $V_{DD}$ where the NCFET exhibits sufficient delay.

## 6.3 Iso-Performance Full-Chip Results at $V_{DD}$ = 0.8 V

Let us consider the $V_{DD}$ = 0.8 V NCFET based iso-performance implementations of the benchmarks at the maximum frequency achieved by baseFET implementation at the same $V_{DD}$ = 0.8 V. Contrary to the 0.4 V analysis in Sec. 5.1, all the viable NCFETs have satisfied the target performance in the 0.8 V analysis as shown in Fig.6.4.

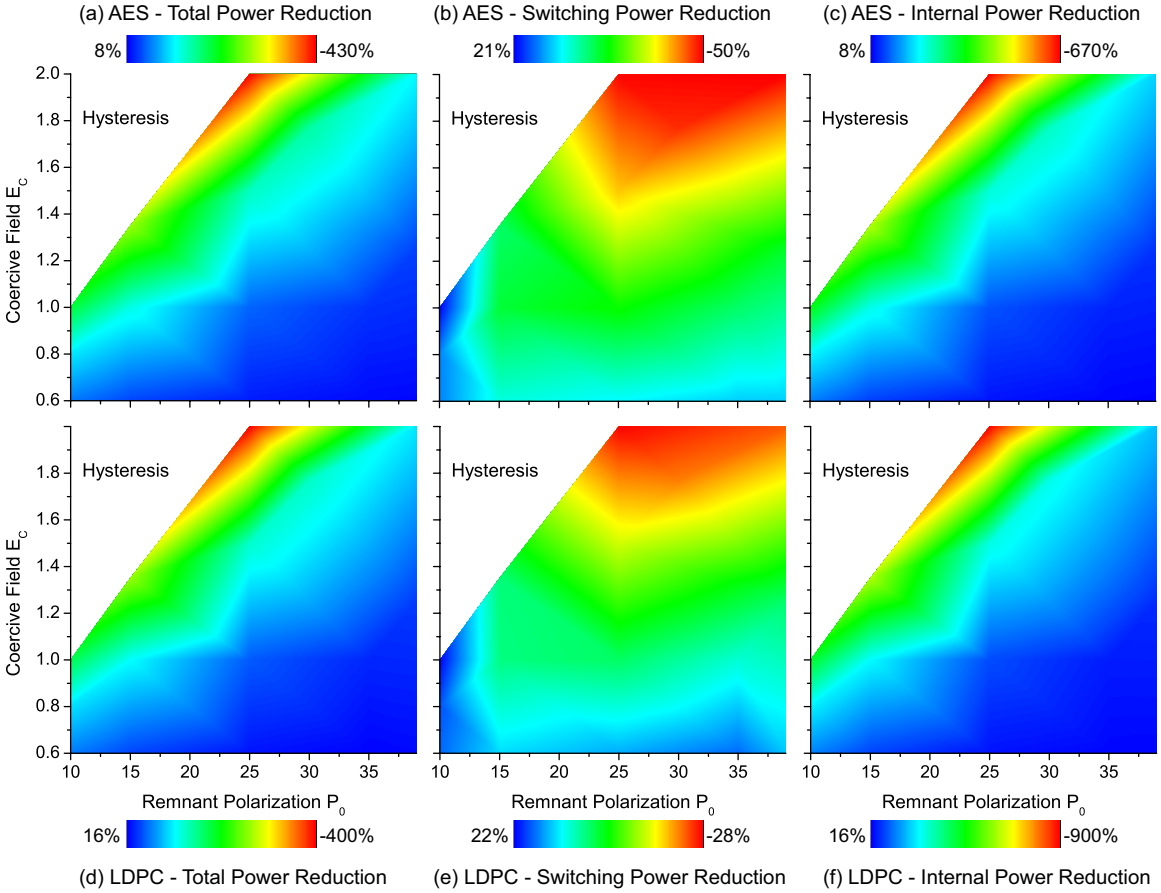



Figure 6.4: Full chip power at $V_{DD}$ = 0.8 V

The full-chip power component characteristics shown in Fig. 6.4 are similar to the 0.8 V inverter power profiles depicted in Fig. 6.2.

- At high $V_{DD}$ = 0.8 V, many NCFETs with low remnant polarization lose negative capacitance enhancement. Therefore, NCFETs in the left consume relatively lower power.

- As a consequence, the region of high switching power NCFETs tilts to the right resembling that of the inverter.

- Very low $|C_{FE}|$ $NCFET_{1;10}$ actually exhibits maximum switching power reduction of 22% owing to the significant decline in capacitance. Whereas high drain current $NCFET_{2;25}$ exhibits maximum switching power deterioration of 50%.

- The extremely low voltage current amplification tremendously increases short-circuit current leading to a maximum of 894% internal power deterioration for $NCFET_{2;25}$. Whereas $NCFET_{0.6;39}$ with very high $|C_{FE}|$ provides 16% and 8% internal power reduction for LDPC and AES respectively.

- Due to the relatively larger variation in internal power, the total power distribution is similar to that of internal power.

- $NCFET_{2;25}$ exhibits the maximum total power deterioration of 430% while $NCFET_{0.6;35}$ yields the maximum total power reduction of 16%.

- The loss of negative capacitance enhancement in low remnant polarization devices causes the maximum internal and total power regions to shrink along the anti-diagonal similar to inverter characteristics.

## 6.4 Maximum Performance Full-Chip Results at $V_{DD}$ = 0.8 V

Fig. 6.5 shows the frequency, power, and EDP distribution for the maximum performance experiments done using NCFETs at $V_{DD}$ = 0.8 V with the following observations.

- The maximum frequency enhancement has reduced from 63% at $V_{DD}$ = 0.4 V to 57% at $V_{DD}$ = 0.8V. This is because the relative current enhancement is lower for all the considered NCFETs either due to loss of negative capacitance in low $|C_{FE}|$ NCFETs or the intrinsically low enhancement in high $|C_{FE}|$ devices.

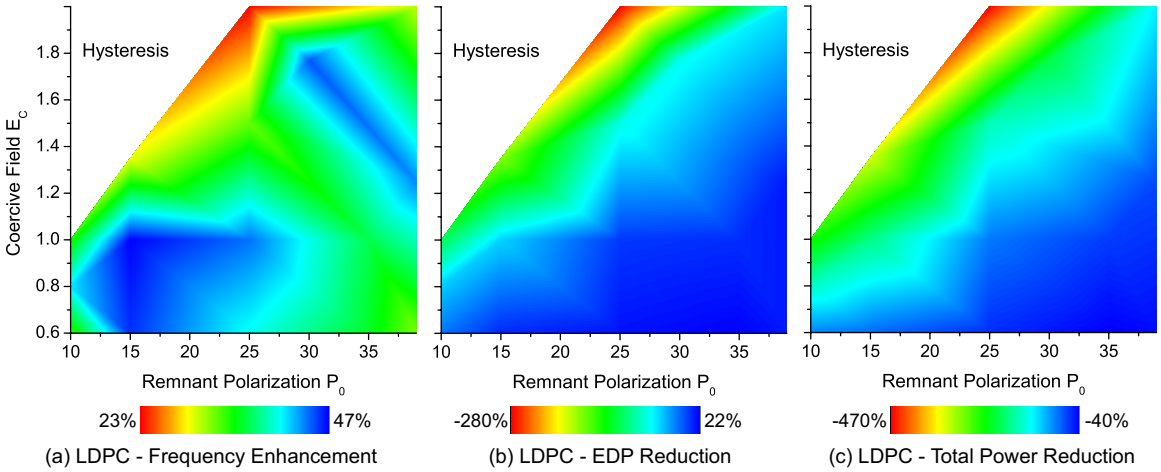



Figure 6.5: NCFET Full chip performance at $V_{DD}$ = 0.8 V

- At $V_{DD}$ = 0.8 V, all the viable NCFETs exhibit low delay and provide a minimum frequency enhancement of 20%.
- Interestingly, $NCFET_{2;25}$ with the highest drain current provides the lowest frequency improvement of 23% for LDPC.
- The high $|C_{FE}|$ NCFETs continue to consume the lowest power and therefore, the minimum power region still remains at the lower right corner. The minimum power consumed is 10% above baseFET since the NCFET and baseFET implementations are done at the same $V_{DD}$ and implemented to meet the maximum frequency.
- Due to the relatively small range of frequency variation and tremendous power consumption, the EDP reduction closely follows the power distribution.

Therefore, the NCFET full-chip power and performance results at $V_{DD}$ = 0.8 V follow the trend estimated from the inverter based simulations. Both power and performance deteriorate for most of the viable NCFETs whereas the performance of very high $|C_{FE}|$ NCFETs improve at high $V_{DD}$.

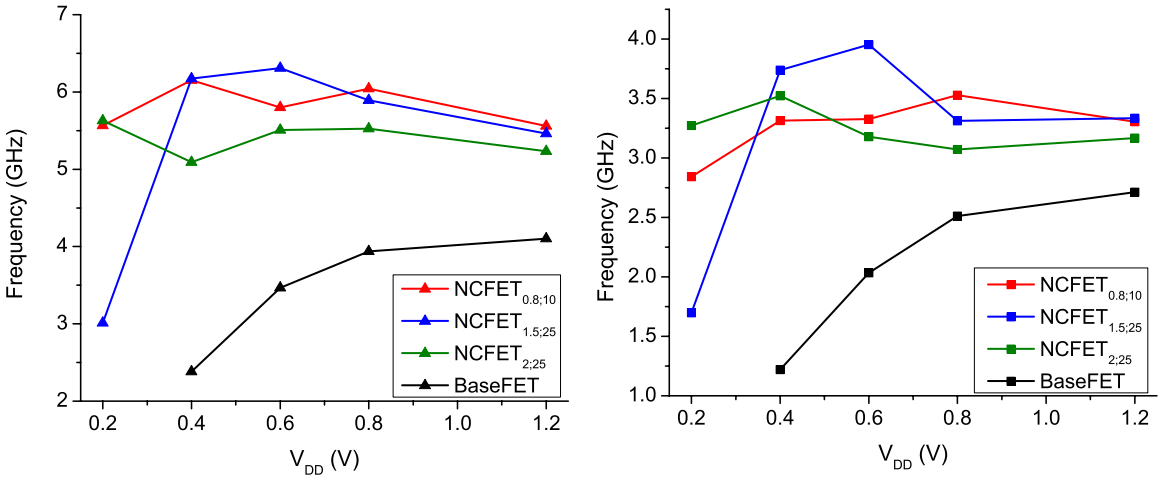



Figure 6.6: NCFET Full-chip performance variation with $V_{DD}$

## 6.5 Full-Chip Results with $V_{DD}$ Variation

Fig. 6.6 shows the maximum frequency achieved by three low $|C_{FE}|$ NCFETs compared to that of baseFET for both the benchmarks as $V_{DD}$ varies between 0.2-1.2 V. The baseFET fails to implement the benchmarks at $V_{DD}$ = 0.2 V and therefore, explored from $V_{DD}$ = 0.4 V. As $V_{DD}$ increases the maximum frequency of baseFET AES and LDPC implementations continue to increase but the rate of change reduces for higher voltages.

The NCFETs exhibit peculiar performance characteristics based on ferroelectric capacitance. Low $|C_{FE}|$ $NCFET_{2;25}$ exhibits tremendous low voltage current amplification and achieves very high frequency for $V_{DD}$ = 0.2 V. In the case of wire-dominated LDPC the performance slightly increases for $V_{DD}$ = 0.4 V and drops for higher voltages owing to the loss of ferroelectric enhancement. Whereas $NCFET_{2;25}$ performance decreases at $V_{DD}$ = 0.4 V due to accumulated gate charge induced high gate capacitance for AES. As $V_{DD}$ further increases, the gate capacitance also decreases leading to the trend in Fig. 6.6.

$NCFET_{0.8;10}$ exhibits relatively higher current enhancement and increases performance as $V_{DD}$ increases from 0.2-0.8 V. High $|C_{FE}|$ $NCFET_{1.5;25}$ exhibits very low frequency at $V_{DD}$ = 0.2 V due to low drain current and provides peak performance at $V_{DD}$ = 0.6 V.

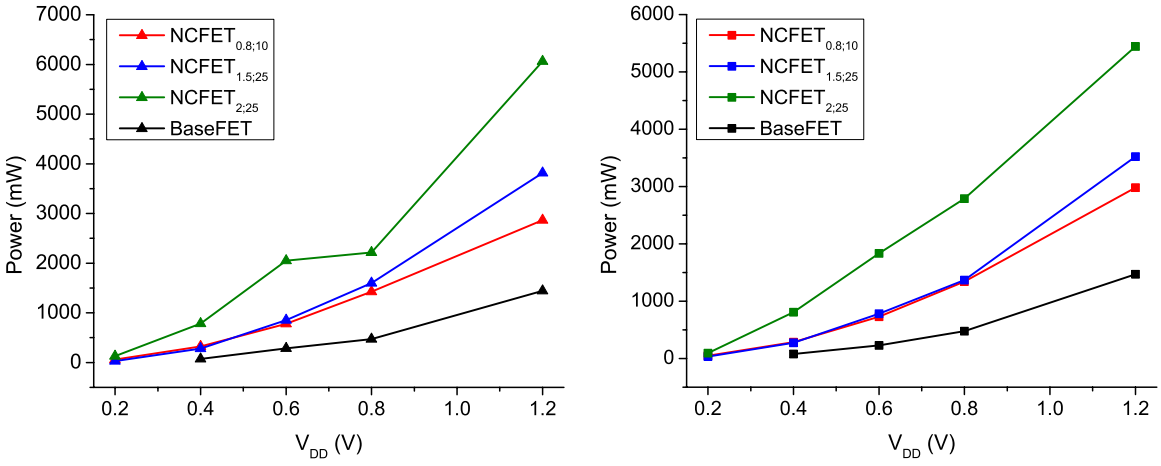



Figure 6.7: NCFET Full-chip power variation with $V_{DD}$

Fig. 6.7 shows the total power consumption of the maximum performance implementations discussed above as $V_{DD}$ increases from 0.2 V to 1.2 V.

- All the implementations exhibit significant surge in power consumption as $V_{DD}$ increases from 0.2 V to 1.2 V.
- The NCFET power consumptions are higher than corresponding baseFET consumptions due to negative capacitance induced current enhancement.
- $NCFET_{2;25}$ with the maximum drain current exhibits the highest power consumption.
- For low $V_{DD}$ $NCFET_{0.8;10}$ and $NCFET_{1.5;25}$ exhibit similar power consumption. Whereas the former exhibits lower power consumption at high $V_{DD}$ due to low $P_0$.

Therefore, the performance and power consumption of NCFETs are primarily determined by the associated ferroelectric parameters and operating voltage. For maximum power reduction or performance at a given voltage there exists a set of optimal ferroelectric parameter combinations and vice versa.

# CHAPTER 7

# CONCLUSIONS

Negative Capacitance Field Effect Transistor (NCFET) offers tremendous power reduction and frequency enhancement resulting in more than a node improvement with the same geometric dimensions. It is shown that the NCFET with the lowest sub-threshold slope does not exhibit the highest power reduction or frequency enhancement owing to higher drain current and capacitance. The NCFET power consumption depends on gate capacitance, short-circuit current, and gate-overdrive voltage whereas the performance enhancement depends on relative current and capacitance enhancement. Therefore, the power and performance characteristics of NCFET devices are primarily determined by ferroelectric parameters and operating voltage. The basic inverter behavior is shown to effectively predict the full-chip power and performance characteristics at various operating voltages. The comprehensive multi-level multi-voltage analysis leads to the following design guideline: each NCFET with given ferroelectric properties are associated with an optimal operating voltage and at a given operating voltage a set of NCFETs with optimal ferroelectric parameters exist to maximize performance enhancement and/or power reduction. Thus, the tremendous power and performance optimization capability coupled with low fabrication overhead make NCFET the most favorable alternative CMOS technology. The exhaustive power and performance analyses in this work will aid device and circuit designers in selecting optimal parameters and $V_{DD}$. This work can be further extended by exploring individual NCFET fabrication data based models and libraries, multi-$V_{TH}$ library development for low-power and multi-frequency analysis, interconnect technology with negative capacitance support, and multi-corner multi-mode analysis.

## REFERENCES


[1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano letters*, vol. 8, no. 2, pp. 405–410, 2008.

[2] S. Salahuddin, "Review of negative capacitance transistors," in *2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 2016, pp. 1–1.

[3] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," in *IEDM*, IEEE, 2011, pp. 11–3.

[4] C.-I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, "Effects of the variation of ferroelectric properties on negative capacitance FET characteristics," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2197–2199, 2016.

[5] S. Khandelwal, A. I. Khan, J. P. Duarte, A. B. Sachid, S. Salahuddin, and C. Hu, "Circuit performance analysis of negative capacitance FinFETs," in *2016 IEEE Symposium on VLSI Technology*, 2016.

[6] A. Aziz, S. Ghosh, S. Datta, and S. K. Gupta, "Physics-based circuit-compatible spice model for ferroelectric transistors," *IEDL*, vol. 37, no. 6, pp. 805–808, 2016.

[7] S. K. Samal, S. Khandelwal, A. I. Khan, S. Salahuddin, C. Hu, and S. K. Lim, "Full chip power benefits with negative capacitance FETs," in *IEEE/ACM ISLPED*, 2017, pp. 1–6.

[8] K.-S. Li, P. G. Chen, T. Y. Lai, C. H. Lin, C. C. Cheng, C. C. Chen, Y. J. Wei, Y. F. Hou, M. H. Liao, M. H. Lee, M. C. Chen, J. M. Sheih, W. K. Yeh, F. L. Yang, S. Salahuddin, and C. Hu, "Sub-60mv-swing negative-capacitance FinFET without hysteresis," in *IEDM*, IEEE, 2015, pp. 22–6.

[9] Z Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J. Liu, J. Shi, H. J. Kim, R. Sporer, C. Serrao, A. Busquet, P. Polakowski, J. Mller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEDM*, IEEE, 2017.

[10] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and compact modeling of negative capacitance transistor with

high on-current and negative output differential resistance," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4986–4992, 2016.

[11] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *IEDL*, vol. 38, no. 9, pp. 1328–1330, 2017.

[12] S. Khandelwal, J. P. Duarte, A. Medury, Y. S. Chauhan, and C. Hu, "New industry standard FinFET compact model for future technology nodes," in *Symposium on VLSI Technology*, 2015, T62–T63.

[13] "ITRS 2015, http://www.itrs2.net/itrs-reports.html," accessed Oct-2017.

[14] M. Martins, J. M. Matos, R. P. Ribas, A. Reis, G. Schlinker, L. Rech, and J. Michelsen, "Open cell library in 15nm FreePDK technology," in *Proceedings of the International Symposium on Physical Design*, ACM, 2015, pp. 171–178.

[15] T. Böscke, J Müller, D Bräuhaus, U Schröder, and U Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, p. 102 903, 2011.

[16] T Olsen, U Schröder, S Müller, A Krause, D Martin, A Singh, J Müller, M Geidel, and T Mikolajick, "Co-sputtering yttrium into hafnium oxide thin films to produce ferroelectric properties," *Applied Physics Letters*, vol. 101, no. 8, p. 082 905, 2012.

[17] M. Hyuk Park, H. Joon Kim, Y. Jin Kim, W. Lee, T. Moon, and C. Seong Hwang, "Evolution of phases and ferroelectric properties of thin hf0. 5zr0. 5o2 films according to the thickness and annealing temperature," *Applied Physics Letters*, vol. 102, no. 24, p. 242 905, 2013.

[18] M Hoffmann, U Schroeder, T Schenk, T Shimizu, H Funakubo, O Sakata, D Pohl, M Drescher, C Adelmann, R Materlik, *et al.*, "Stabilizing the ferroelectric phase in doped hafnium oxide," *Journal of Applied Physics*, vol. 118, no. 7, p. 072 006, 2015.

[19] T. Böscke, S. Teichert, D Bräuhaus, J Müller, U Schröder, U Böttger, and T Mikolajick, "Phase transitions in ferroelectric silicon doped hafnium oxide," *Applied Physics Letters*, vol. 99, no. 11, p. 112 904, 2011.

[20] J Müller, T. Böscke, D Bräuhaus, U Schröder, U Böttger, J Sundqvist, P Kücher, T Mikolajick, and L Frey, "Ferroelectric zr0. 5hf0. 5o2 thin films for nonvolatile memory applications," *Applied Physics Letters*, vol. 99, no. 11, p. 112 901, 2011.

[21] J Müller, U Schröder, T. Böscke, I Müller, U Böttger, L Wilde, J Sundqvist, M Lemberger, P Kücher, T Mikolajick, *et al.*, "Ferroelectricity in yttrium-doped hafnium oxide," *Journal of Applied Physics*, vol. 110, no. 11, p. 114 113, 2011.

[22] S Mueller, C Adelmann, A Singh, S Van Elshocht, U Schroeder, and T Mikolajick, "Ferroelectricity in gd-doped hfo2 thin films," *ECS Journal of Solid State Science and Technology*, vol. 1, no. 6, N123–N126, 2012.

[23] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, "Incipient ferroelectricity in al-doped hfo2 thin films," *Advanced Functional Materials*, vol. 22, no. 11, pp. 2412–2417, 2012.

[24] J. Muller, T. S. Boscke, U. Schroder, S. Mueller, D. Brauhaus, U. Bottger, L. Frey, and T. Mikolajick, "Ferroelectricity in simple binary zro2 and hfo2," *Nano letters*, vol. 12, no. 8, pp. 4318–4323, 2012.

[25] J Muller, T. Boscke, S Muller, E Yurchuk, P Polakowski, J Paul, D Martin, T Schenk, K Khullar, A Kersch, *et al.*, "Ferroelectric hafnium oxide: A cmos-compatible and highly scalable approach to future ferroelectric memories," in *Electron Devices Meeting (IEDM), 2013 IEEE International*, IEEE, 2013, pp. 10–8.

[26] M. Pešić, M. Hoffmann, C. Richter, T. Mikolajick, and U. Schroeder, "Nonvolatile random access memory and energy storage based on antiferroelectric like hysteresis in zro2," *Advanced Functional Materials*, vol. 26, no. 41, pp. 7486–7494, 2016.

[27] T. Schenk, U. Schroeder, M. Pesic, M. Popovici, Y. V. Pershin, and T. Mikolajick, "Electric field cycling behavior of ferroelectric hafnium oxide," *ACS applied materials & interfaces*, vol. 6, no. 22, pp. 19 744–19 751, 2014.

[28] T. Tromm, J Zhang, J Schubert, M Luysberg, W Zander, Q Han, P Meuffels, D Meertens, S Glass, P Bernardy, *et al.*, "Ferroelectricity in lu doped hfo2 layers," *Applied Physics Letters*, vol. 111, no. 14, p. 142 904, 2017.

[29] M. Hoffmann, T. Schenk, M. Pešić, U. Schroeder, and T. Mikolajick, "Insights into antiferroelectrics from first-order reversal curves," *Applied Physics Letters*, vol. 111, no. 18, p. 182 902, 2017.

[30] G. Karbasian, R. dos Reis, A. K. Yadav, A. J. Tan, C. Hu, and S. Salahuddin, "Stabilization of ferroelectric phase in tungsten capped hf0. 8zr0. 2o2," *Applied Physics Letters*, vol. 111, no. 2, p. 022 907, 2017.

[31] A. Pal, V. K. Narasimhan, S. Weeks, K. Littau, D. Pramanik, and T. Chiang, "Enhancing ferroelectricity in dopant-free hafnium oxide," *Applied Physics Letters*, vol. 110, no. 2, p. 022 903, 2017.

[32] S. J. Kim, D. Narayan, J.-G. Lee, J. Mohan, J. S. Lee, J. Lee, H. S. Kim, Y.-C. Byun, A. T. Lucero, C. D. Young, *et al.*, "Large ferroelectric polarization of tin/hf0. 5zr0. 5o2/tin capacitors due to stress-induced crystallization at low thermal budget," *Applied Physics Letters*, vol. 111, no. 24, p. 242 901, 2017.

[33] S Starschich and U Boettger, "An extensive study of the influence of dopants on the ferroelectric properties of hfo 2," *Journal of Materials Chemistry C*, vol. 5, no. 2, pp. 333–338, 2017.

[34] Y. H. Lee, H. J. Kim, T. Moon, K. Do Kim, S. D. Hyun, H. W. Park, Y. B. Lee, M. H. Park, and C. S. Hwang, "Preparation and characterization of ferroelectric hf0. 5zr0. 5o2 thin films grown by reactive sputtering," *Nanotechnology*, vol. 28, no. 30, p. 305 703, 2017.

[35] P Polakowski, S Riedel, W Weinreich, M Rudolf, J Sundqvist, K Seidel, and J Muller, "Ferroelectric deep trench capacitors based on al: Hfo 2 for 3d nonvolatile memory applications," in *Memory Workshop (IMW), 2014 IEEE 6th International*, IEEE, 2014, pp. 1–4.

[36] Y.-C. Lin, F. McGuire, and A. D. Franklin, "Realizing ferroelectric hf0. 5zr0. 5o2 with elemental capping layers," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 36, no. 1, p. 011 204, 2018.

[37] J Müller, P Polakowski, S Mueller, and T Mikolajick, "Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects," *ECS Journal of Solid State Science and Technology*, vol. 4, no. 5, N30–N35, 2015.